Substrate preparation for selective area growth of III-V nanostructures

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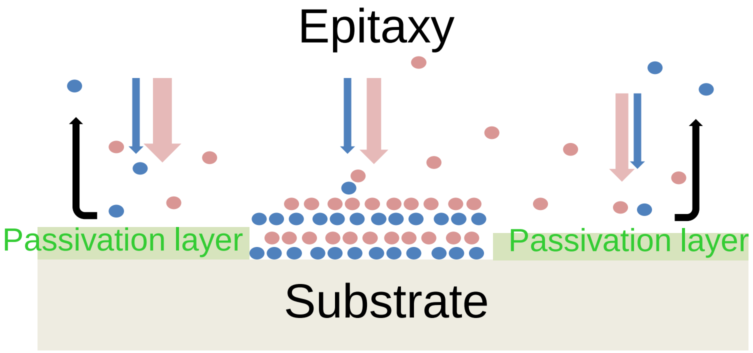
Outline

- Selective Area Growth: definition, motivation and method?
- Opportunities for Selective Area Growth (SAG) for III-V nanostructures
  - Optoelectronics
  - III-V MOSFET development
  - Quantum technologies
- Review of nano-SAG development (mainly MOCVD)
- Development of MBE-SAG for in-plane III-V nanostructures
  - Mask preparation
  - Surface deoxidation
  - Growth conditions
  - Atomic H assisted MBE
  - Examples of III-V nano-SAG using MBE
- Conclusion and prospects

Selective Area Growth (SAG) ?

No deposition on the mask:
no nucleation, diffusion or
re-evaporation?

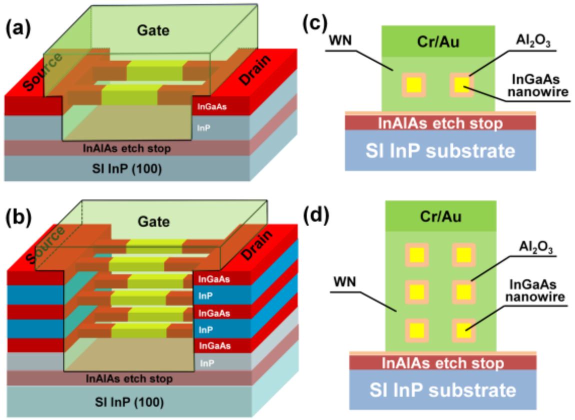


- Selective area growth with respect to a passivation layer (where no deposition occurs)
- Need to open patterns in the passivation layer where the nucleation will happen
- Need to find the conditions for which growth occurs in the patterns whereas no material is deposited on the mask
- Preparation of patterns? Surface inside patterns? What kind of substrate (material, orientation) for what kind of applications?

Why SAG ?

Nanodevice fabrication

- Quantum confinement (nanowires and nanowire arrays)
- Avoid dry etching
- Catalyst free growth
- Position controled nanostructures
- Ease device processing
- Core-shell and in-line heterojunctions

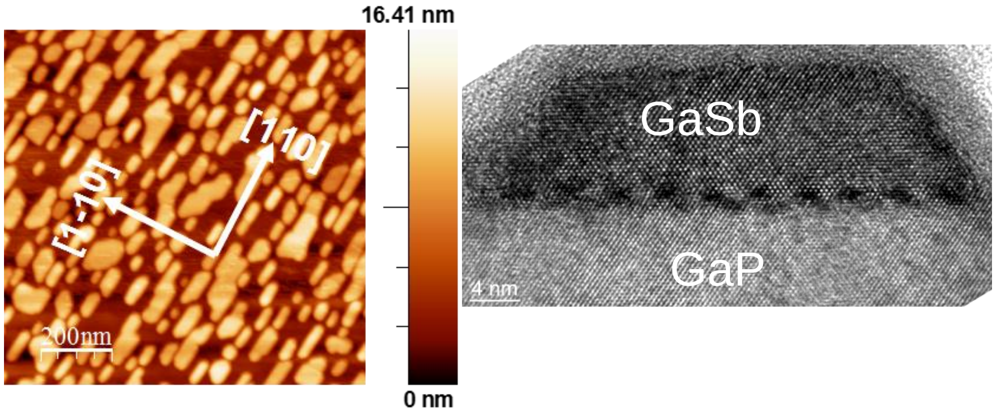


Ex: « 4D MOSFET »

Gu et al, IEEE IEDM (2012)

Accommodate dissimilar materials

- Strain relaxation in nano-islands
- Integration of III-V on Silicon:
  - CMOS ??? (MOSFET, TFET)
  - RF ?
  - Opto ?



Ex: GaSb nano-island on GaP (>11% mismatch) free from TD

S.El Kazzi et al, J. Appl. Phys. 111, 123506 (2012)

How to achieve SAG ?

By Metal Organic Chemical Vapor Deposition (MOCVD) or Chemical Beam Epitaxy (CBE)

☺ Selectivity of Metal organic decomposition between oxyde mask and semiconductor surface

☹ High growth temperature needed for efficient decomposition and to avoid carbon incorporation

By Molecular Beam Epitaxy (MBE) ?

☺ Lower temperature / dopant activation
☺ Carbon incorporation
☹ Selectivity ??
☹ Directivity of the molecular beam (shadow effect)
😐 Temperature control

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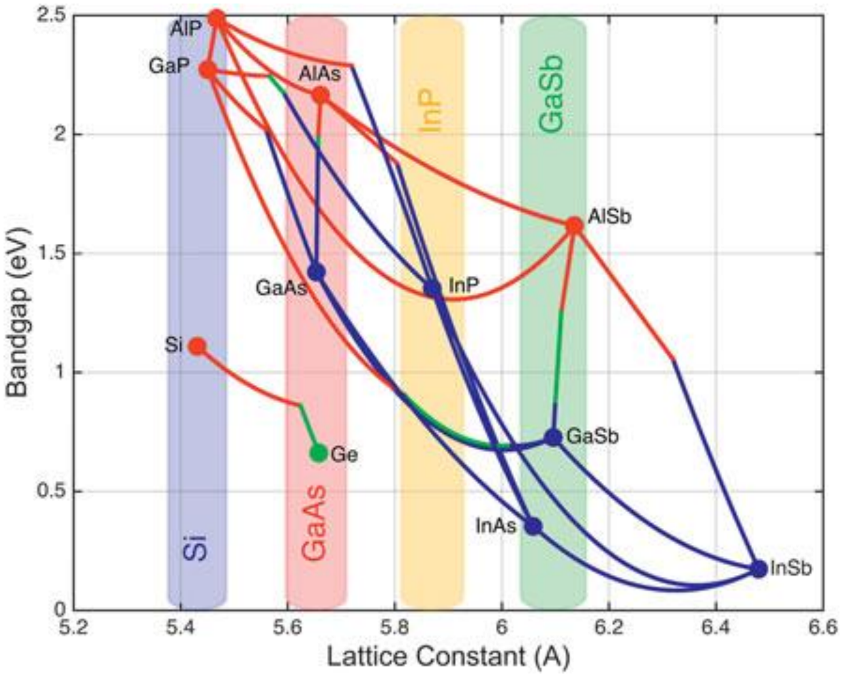
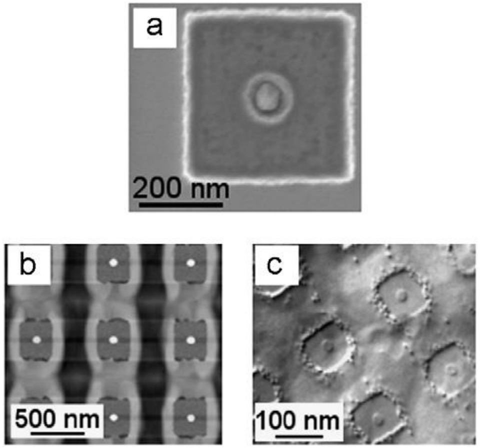
III-V SAG for optoelectronics

- Co-integration of III-V based sources and detectors on CMOS platform



Richardson et al., MRS Bulletin 41, p193 (2016)

- Single photon source emitters ?

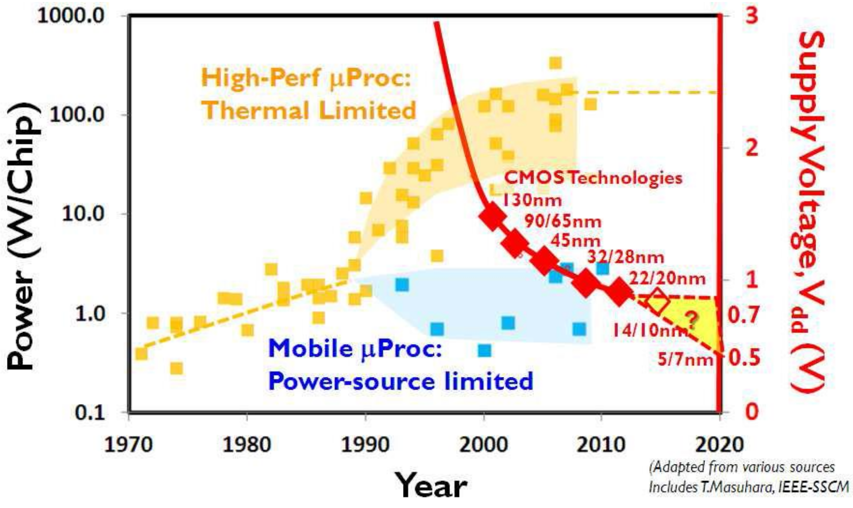


Ex: Single InAs/InP QD grown by SAG

N. Gogneau et al., JCG 310 (2008) 3143

III-V SAG for microelectronics

Si-based CMOS supply voltage reaches a threshold



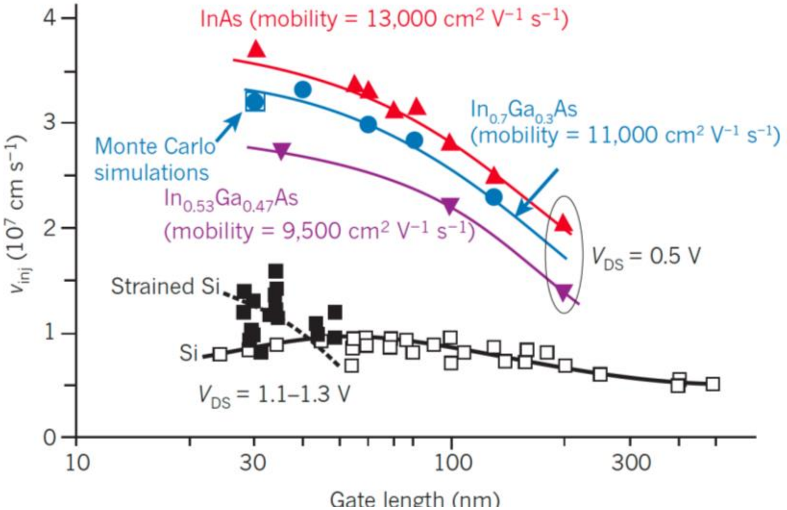
(Adapted from various sources
Includes T.Masuhara, IEEE-SSCM 2013)

N.Collaert (IMEC), ESSDERC'2015

How to reduce V_{dd} while keeping large ON-current?

$$I_D = q\, n_{charge}\, v_{inj}$$

$V_{inj(InGaAs)} > 2V_{inj}(Si)$ at less than half *VDD !*



J.Del Alamo, Nature 479, 318 (2011)

<u>Challenges for III-V CMOS</u>:

- Fundamental issues: Low DOS in low effective mass material => degradation of gate control efficiency
  Quantum confined nanostructures and high-k dielectrics are needed.

- Technological issues: nanoscale fabrication and co-integration with pMOS (Ge?) on Si (001)
  low thermal budget, gate length < 20 nm, low resistance ohmic contacts, low parasitic capacitances

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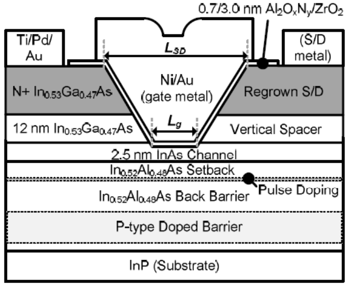
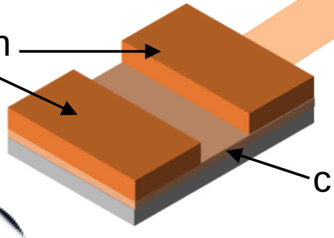
Architecture for efficient In(Ga)As MOSFET

Complexity
Gate command efficiency



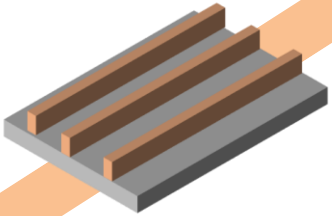
Ex: InAs QW MOSFET with MOCVD InGaAs RSD (UCSB)
S.Lee et al, VLSI 2014

2D QW channel with RSD

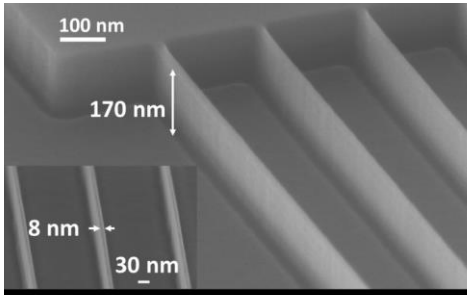


n+ regrown contacts

channel

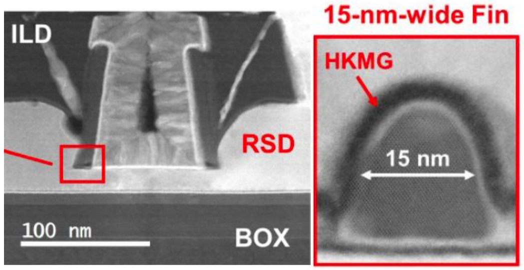


FinFET



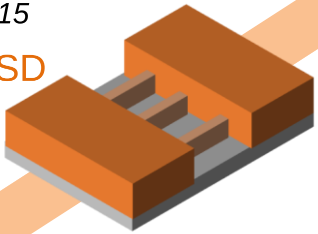
Top-down InGaAs FinFET fabrication by RIE +digital etching (MIT)
Vardi et al, EDL 2016

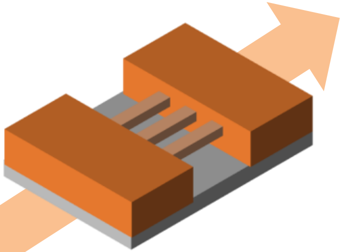
InGaAs FinFET on Si: mixed top-down (Fin fabrication) and bottom-up (MOCVD raised SD contacts) process (IBM)



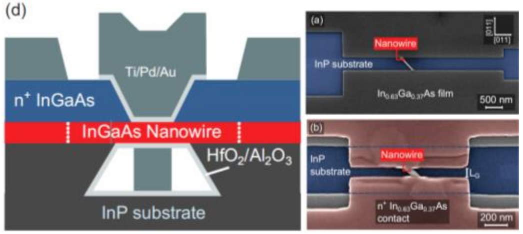
Djara et al, EDL 2015

FinFET with RSD





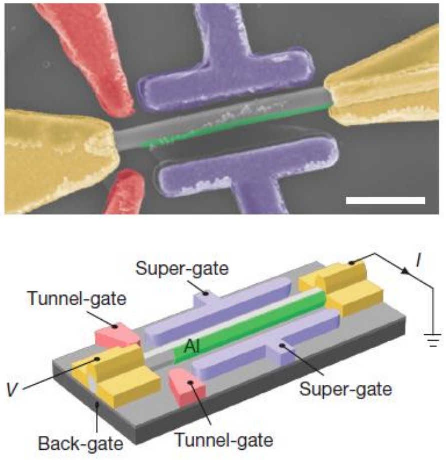
NW FET with gate all around (GAA) and RSD



Single Suspended InGaAs Nanowire MOSFET with RSD (Univ. Lund)

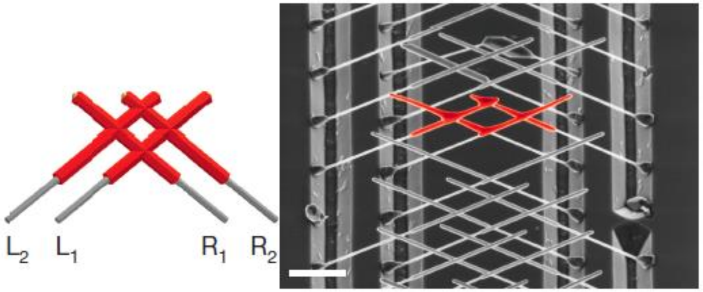
Zota et al, IEDM 2015

III-V SAG for quantum technologies ?



H.Zhang et al, Nature 556, p. 74 (2018)

- Majorana fermions in 1D semiconductor with large spin-orbit coupling (InSb, InAs) nanowire <u>proximity coupled with a superconductor</u>



Ex: Elaboration of InSb NW networks by VLS

Nature 548 p434 (2017)

- Needs for branched ballistic nanostructures for complex quantum circuit architectures

Devices based on VLS growth + transfer on a host substrate:

Interest of SAG for position controlled nanowires and nano-crosses and avoid gold assisted growth

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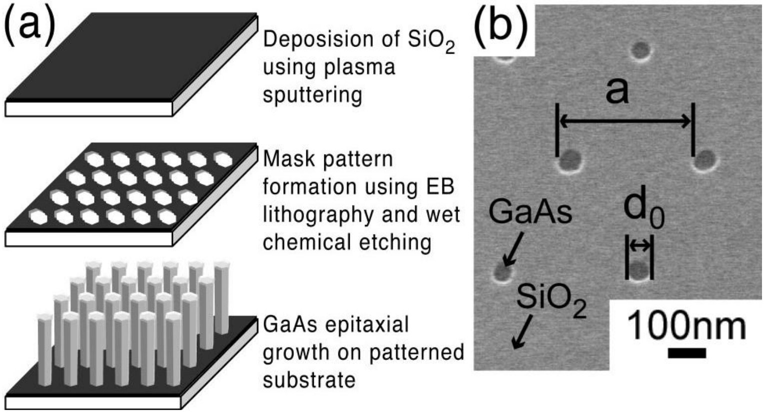
III-V integration on Silicon using nano-SAG

III-V integration on Silicon using SAG

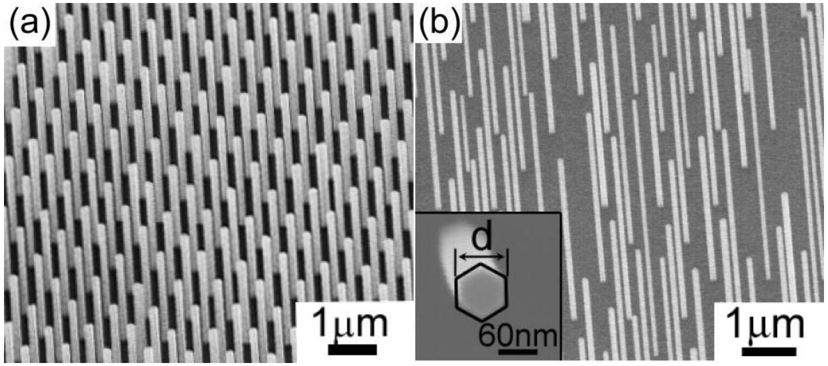
Vertical NW on Si (111): SAG or VLS ?

- GaAs on Si (111)



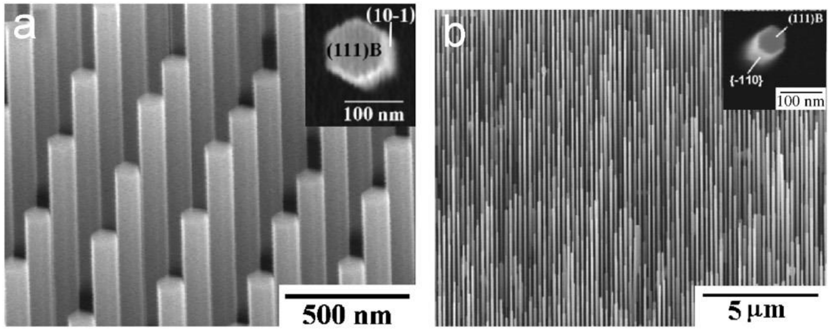
200 nm holes

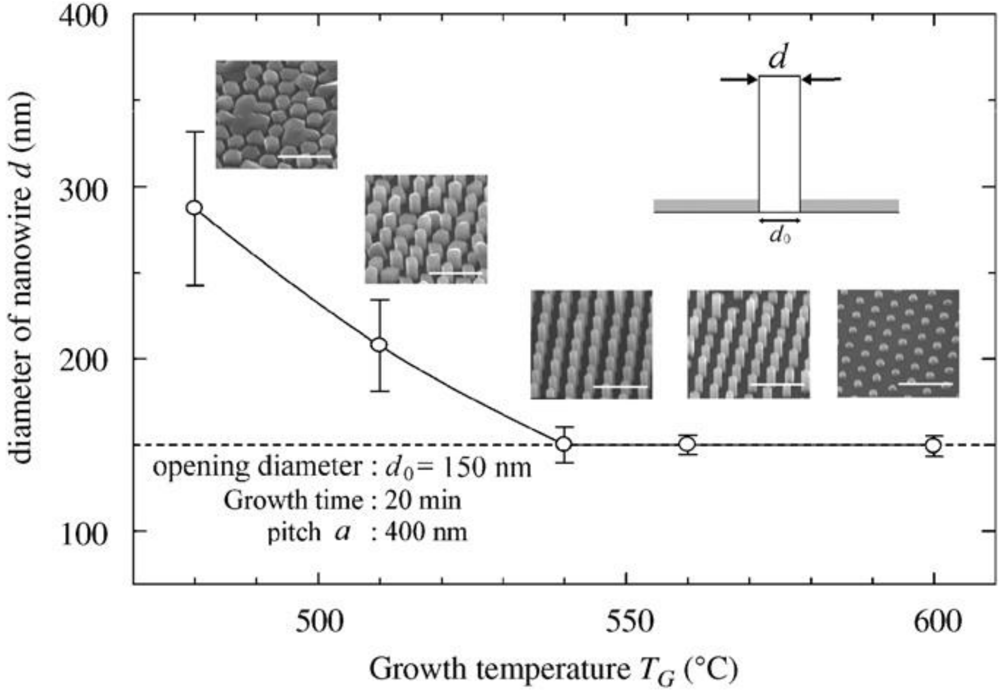
50 nm holes



Noborisaka et al, Appl. Phys. Lett. 86, 213102 (2005)

- InAs on Si (111)



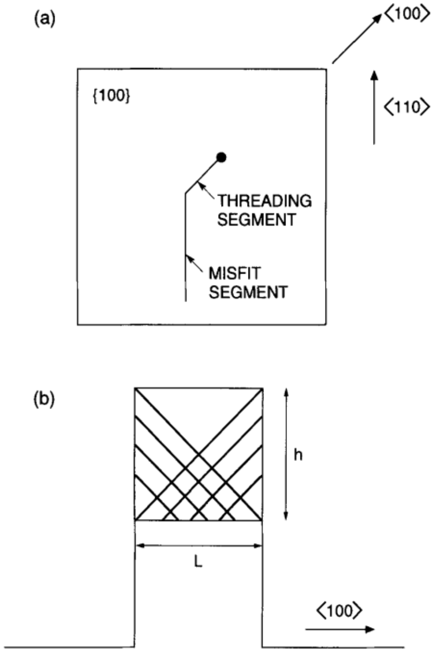


Tomioka et al, JCG 298 (2007) 644–647

III-V integration on Silicon using SAG

Threading dislocation filter using aspect ratio trapping (ART)

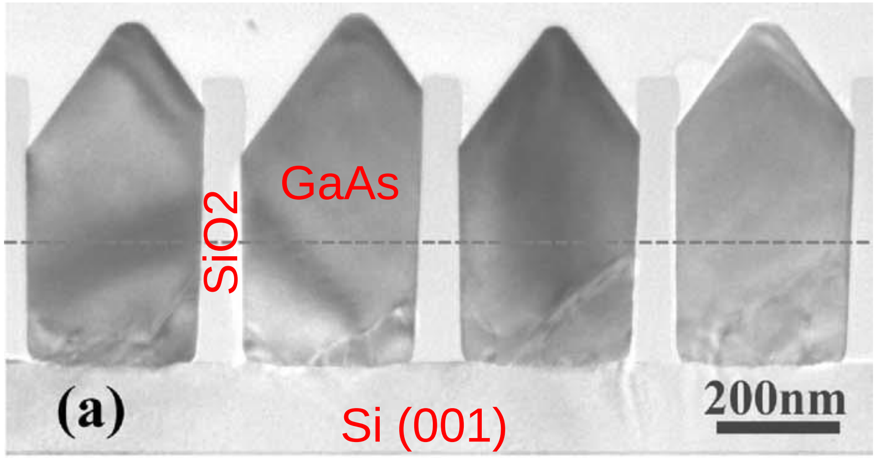
Idea: blocking the threading dislocations propagating in (111) planes by SiO_2 sidewalls



E. A. Fitzgerald et al, J. Electronic Materials 20, p. 839 (1991)

Micro-scale

GaAs on Si (001)

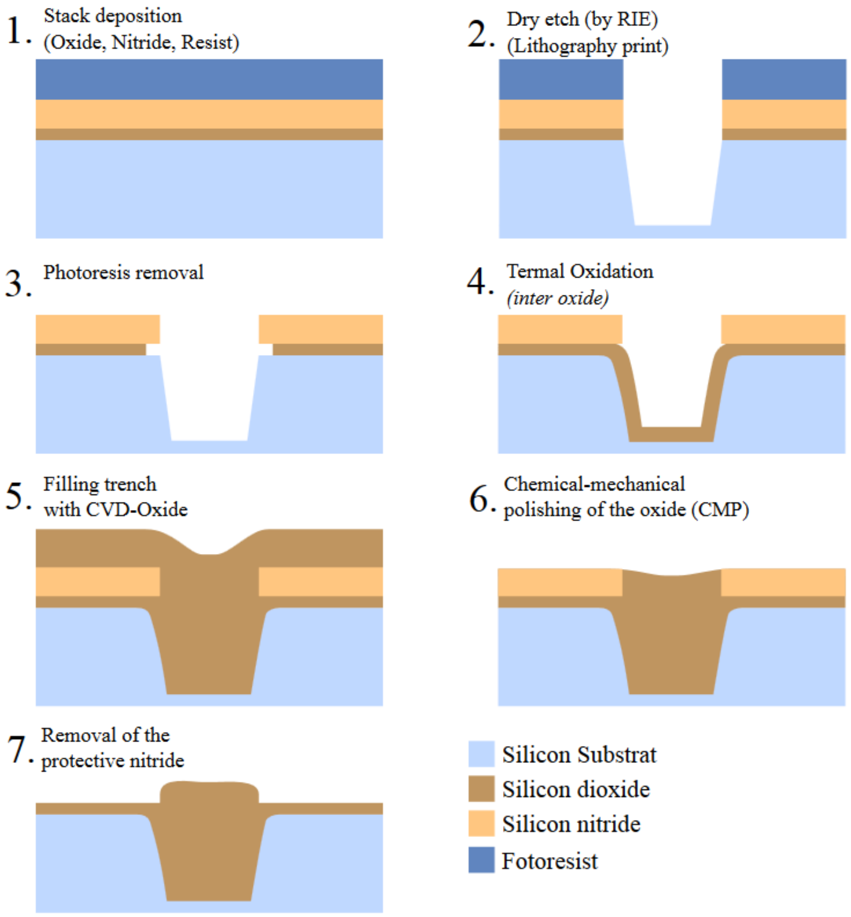


Li et al, Appl. Phys. Lett. 91, 021114 (2007)

Nano-scale

III-V integration on Silicon using SAG

Aspect Ratio Trapping using Shalow Trench Isolation process developed for CMOS technology



https://upload.wikimedia.org/wikipedia/commons/e/e2/Shallow_trench_isolation_process.svg

- Process developed for 250 nm nodes and below
- Optical lithography (immersion)
- Trenches as narrow as 20 nm for a SiO_2 thickness of 250 nm can be achieved on 300 mm wafers
- Dense patterns can be obtained
- Silicon is etched between the trenches using vapor HCl

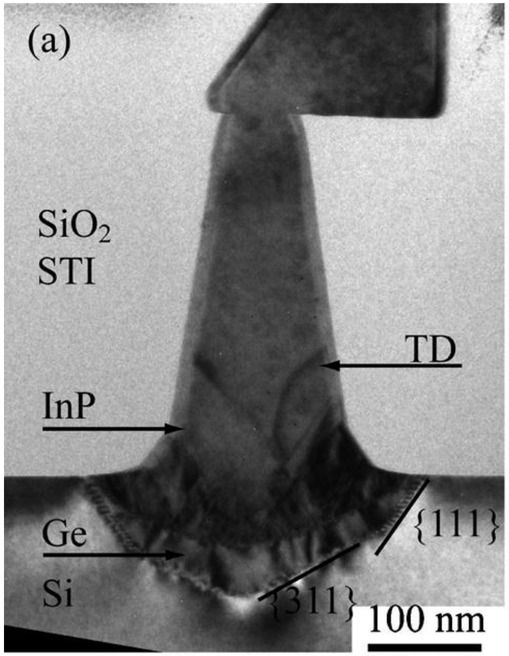
III-V integration on Silicon using SAG

Aspect Ratio Trapping using Shalow Trench Isolation:

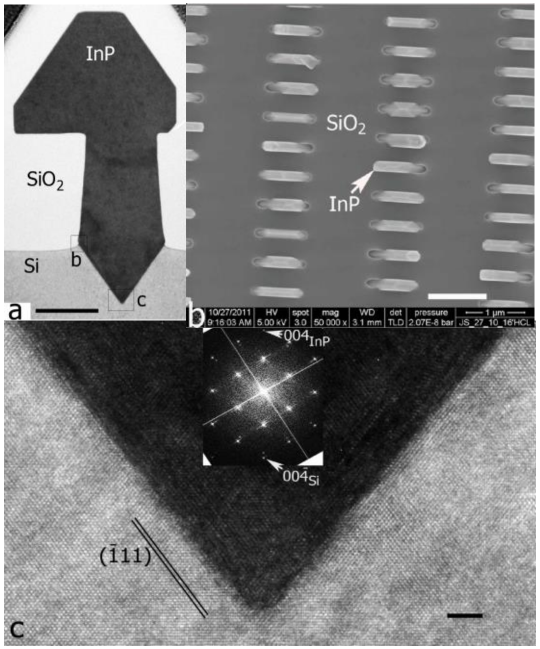
Impact of Si surface preparation for InP deposition (IMEC)

- Si native oxide inside trenches removed using SiCoNi process:
  High temperature bake above 800ºC in H_2 at 50 millibars

- « Rounded » Ge deposit before InP growth or $(111)_{Si}$ V-surface before InP growth (etched with TMAH or KOH @ 70° C)



Wang et al, Appl. Phys. Lett. **97**, 121913 (2010)

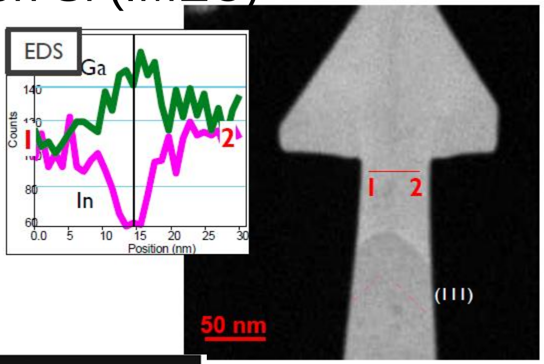


Paladugu et al, Cryst. Growth Des. 12, p. 4696−4702 (2012)

III-V integration on Silicon using SAG

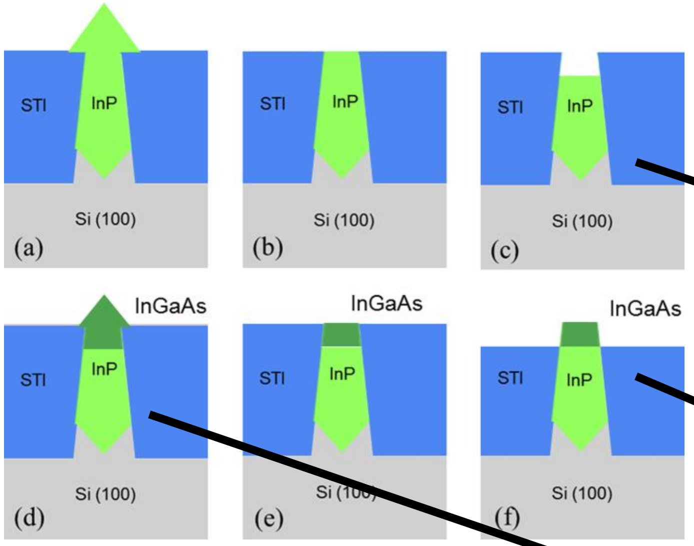
Aspect Ratio Trapping using Shalow Trench Isolation:

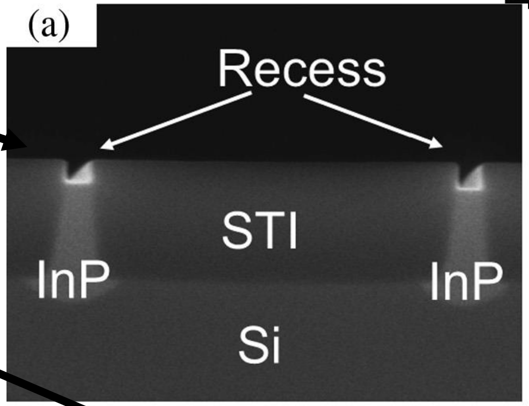
InGaAs in-plane nanowire MOSFET fabrication on Si (IMEC)

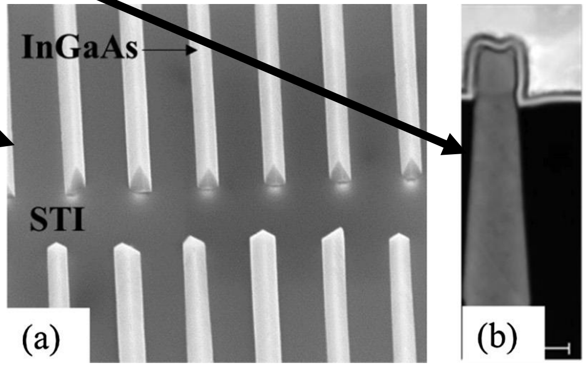


Merckling, SEMICON Europa (2016)

- ➢ InP SAG + CMP + InGaAs SAG to avoid ternary InGaAs stoichiometry variation at inter-facets region when growth is initiated on (111) InP facets







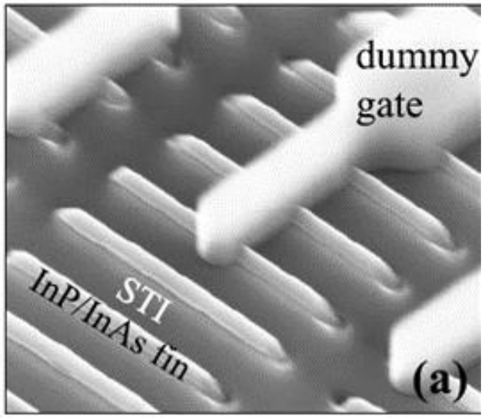
Waldron et al, Solid-State Electronics 115, p81 (2016)

III-V integration on Silicon using SAG

Aspect Ratio Trapping using Shalow Trench Isolation:

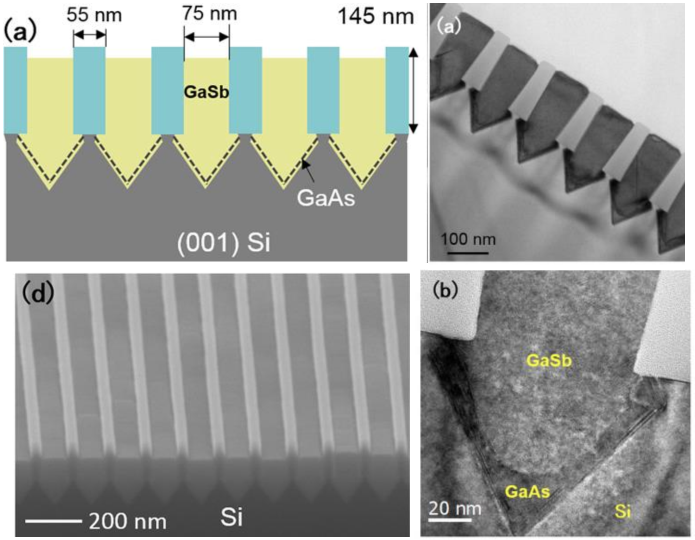
Other III-V materials

- InAs on InP on Si



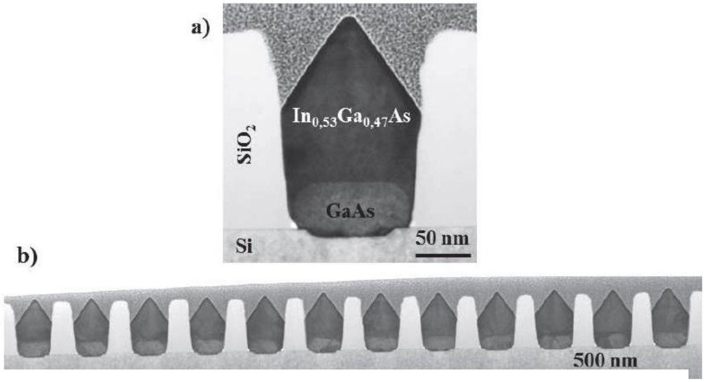
Doornbos et al, JEDS 4, p253 (2016)

- GaSb on GaAs on Si



Li et al, Appl. Phys. Lett. 111, 172103 (2017)

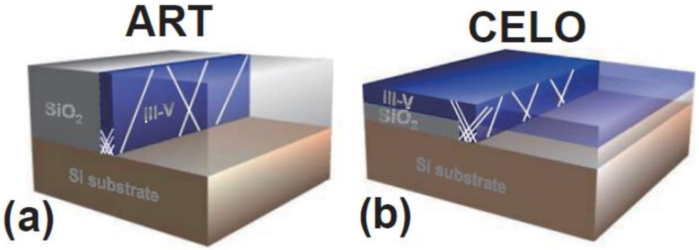
- InGaAs on GaAs on Si



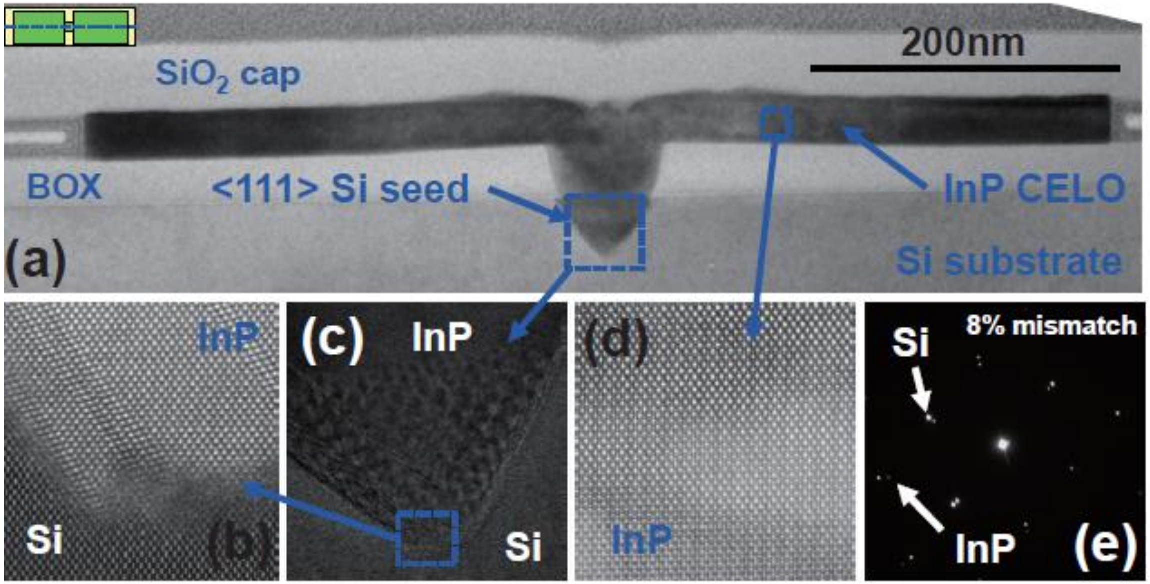
R.Cipro (LTM), thèse Univ. Grenoble Alpes (2016)

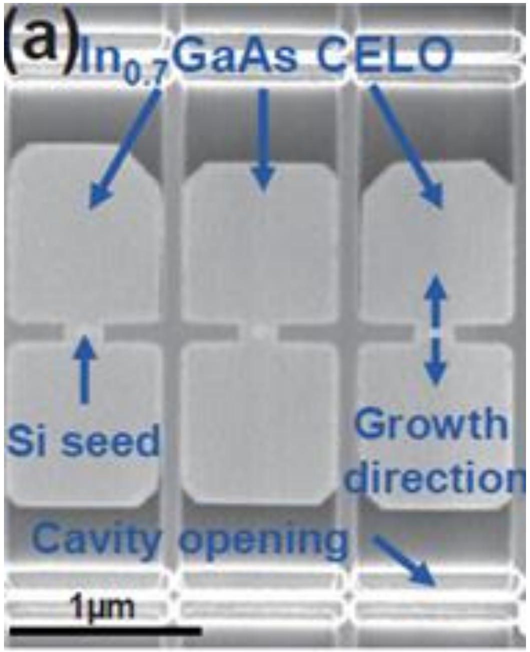
III-V integration on Silicon using SAG

Confined Epitaxial Lateral Overgrowth (CELO) developed by IBM



Czonormaz et al (IBM) , VLSI (2015)





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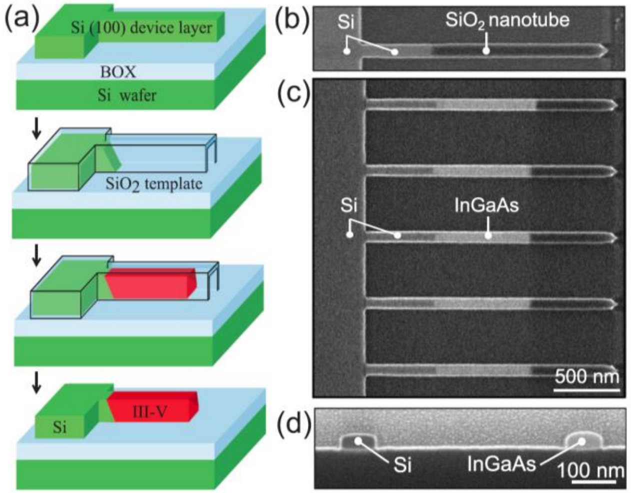
III-V integration on Silicon using SAG

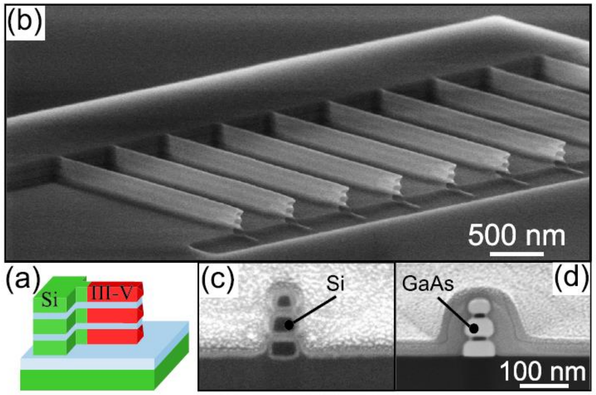
Template Assisted Epitaxy (TASE) developed by IBM

- InGaAs in-plane NW on Si

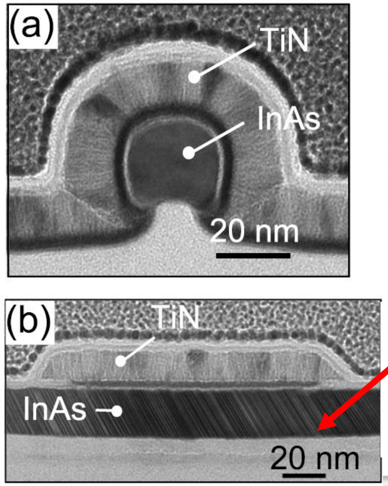


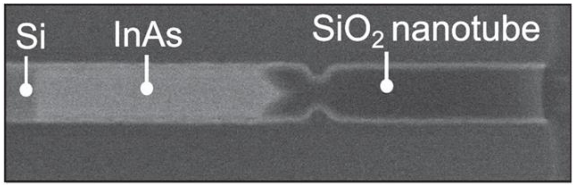
Schmidt et al, Appl. Phys. Lett. 106, 233101 (2015)

- Super-imposed GaAs in-plane NW on Si



- Gate all-around InAs NW MOSFET on Si

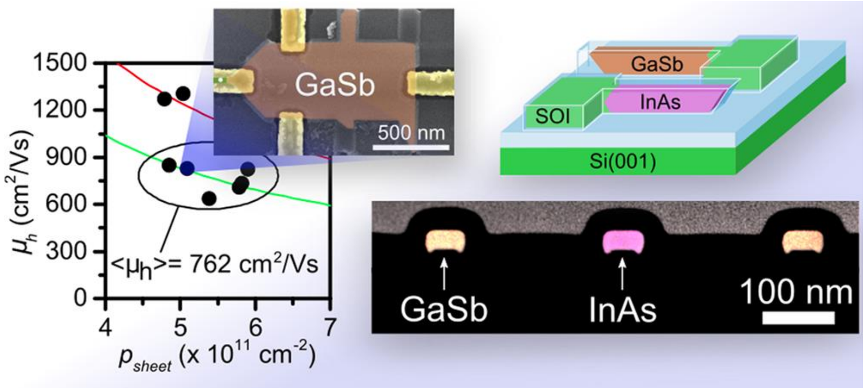




μ_{Hall}=5400 cm^2/V.s.

Large density of stacking fault due to growth on (111) planes

- High mobility GaSb on Si and co-integration with InAs

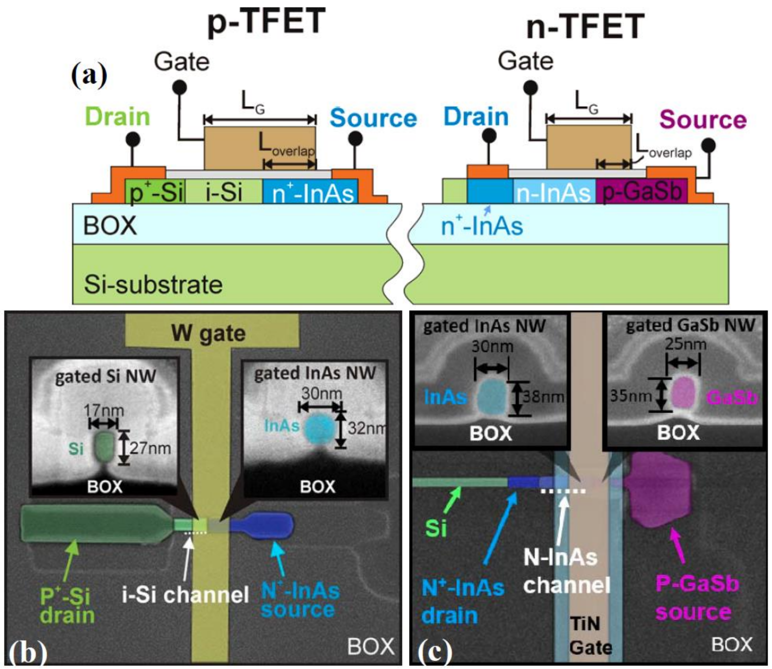


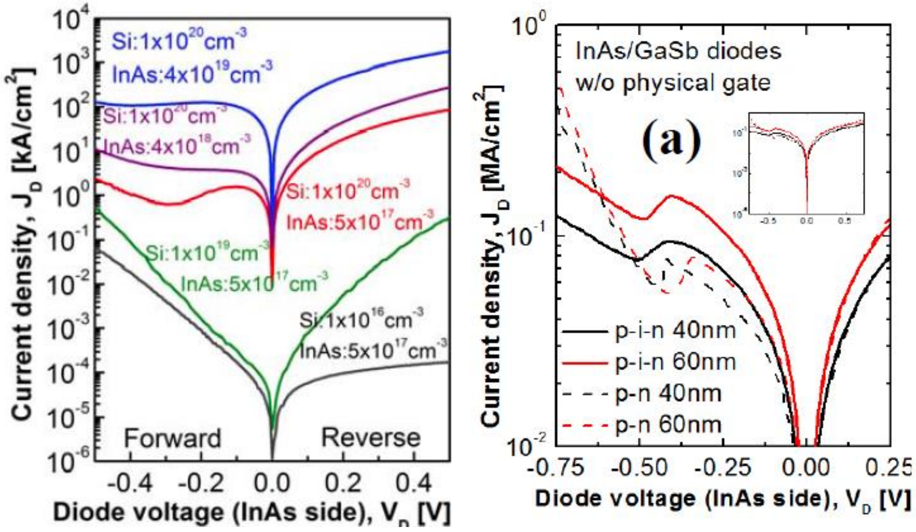
Borg et al, ACS Nano 2017, 11, 2554−2560

III-V integration on Silicon using SAG

Template Assisted Epitaxy (TASE) developed by IBM

- InAs/Si and GaSb/InAs in-plane heterojunctions for TFET fabrication



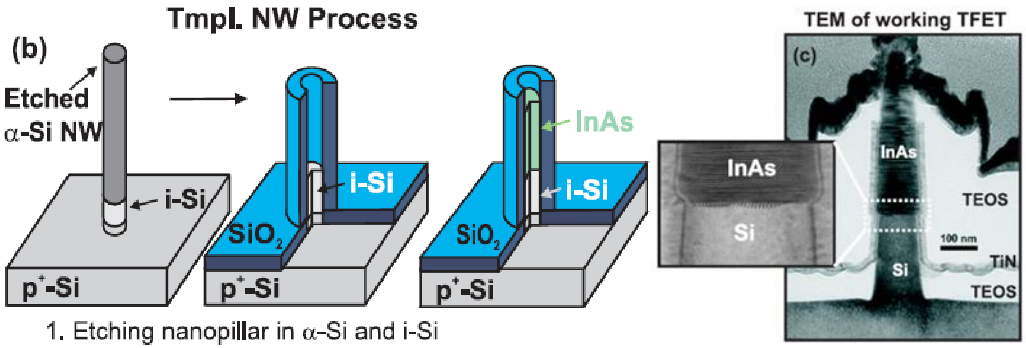


Cutaia et al, VLSI (2016)

III-V integration on Silicon using SAG

Template Assisted Epitaxy (TASE) of vertical NW

- InAs/Si vertical heterojunctions (IBM - MOCVD)

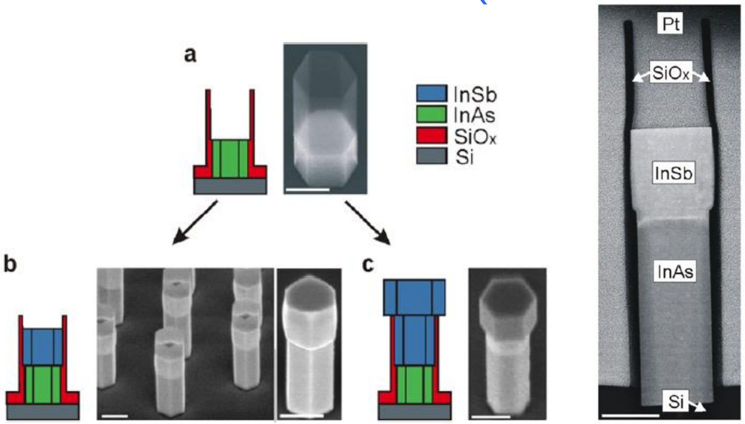


1. Etching nanopillar in α-Si and i-Si
2. Create oxide template around NW and etch α-Si.
3. Grow InAs inside template & strip SiO_x template

Cutaia et al, JEDS 3, p176 (2015)

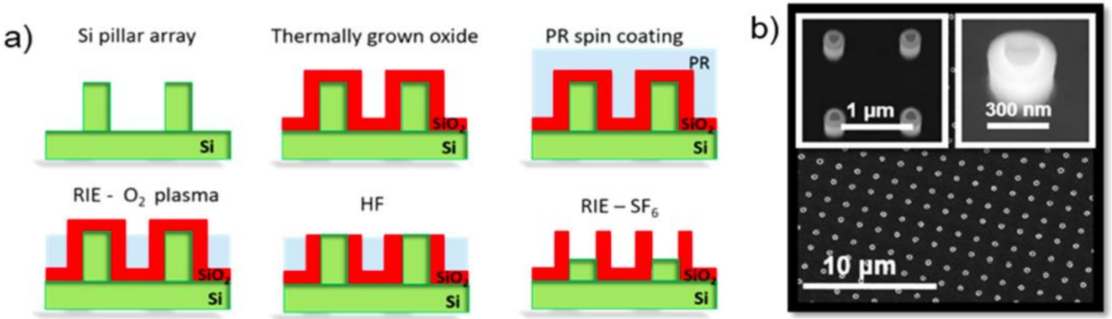
Substrats Si (111)

- InSb/InAs/Si vertical NW (IBM - MOCVD)



Kanungo et al, Nanotechnology 24 (2013) 225304

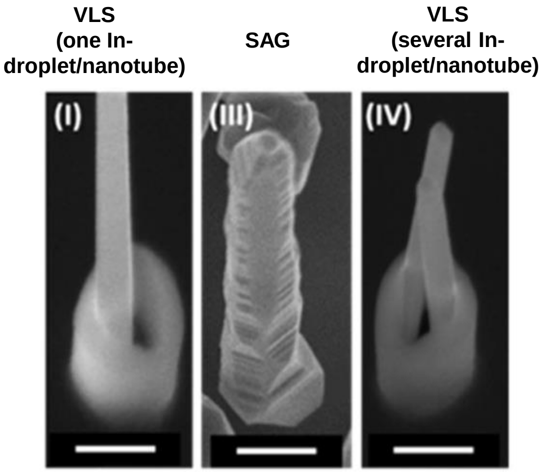
- InAs/Si vertical NW (EPFL – MBE VLS)



Substrats Si (111)

Before introduction into the MBE growth chamber, samples were dipped for 2 s in poly-silicon etch solution [HNO3(70%):HF(49%):H2O]

J Vukajlovic-Plestina et al, Nanotechnology 27 (2016) 455601



High yield Low yield Low yield

Impact of growth mode on yield

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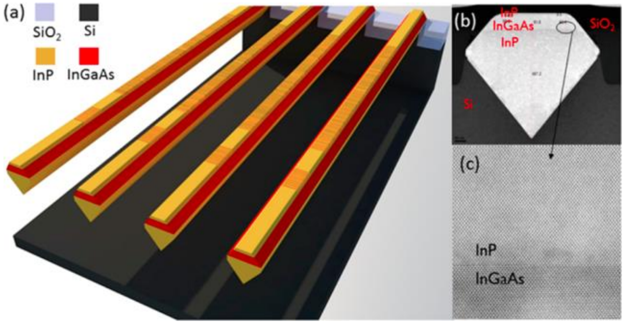
III-V integration on Silicon using SAG

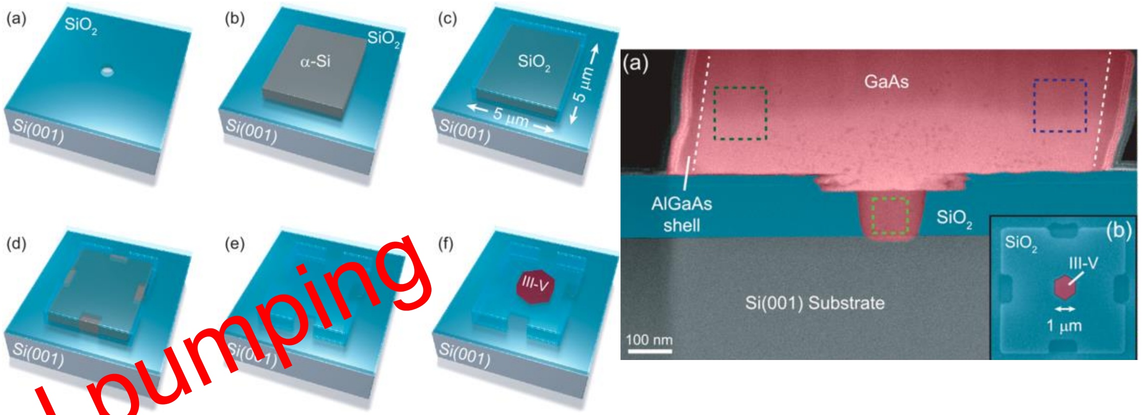
What about optoelectronic applications?

- InP and InGaAs/InP DFB laser integrated on Si using ART (IMEC)



Tian et al, Nano Lett. 17, 559−564 (2017)
Wang et al, Nature Photonics 9, 838 (2015)

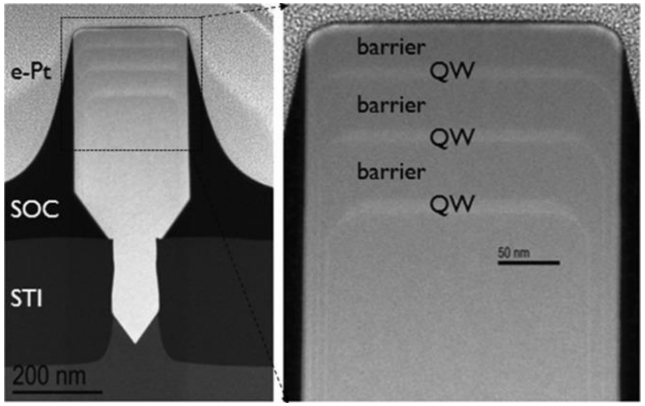
- AlGaAs/GaAs µ-disk laser on Si using TASE (IBM)



Wirths et al, ACS Nano 2018, 12, 2169−2175

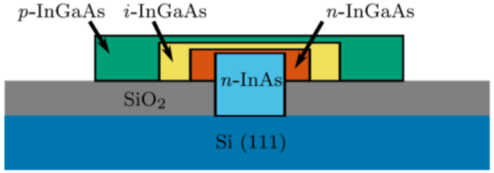
Optical pumping

- InGaAs/GaAs laser integrated on Si using ART (IMEC)

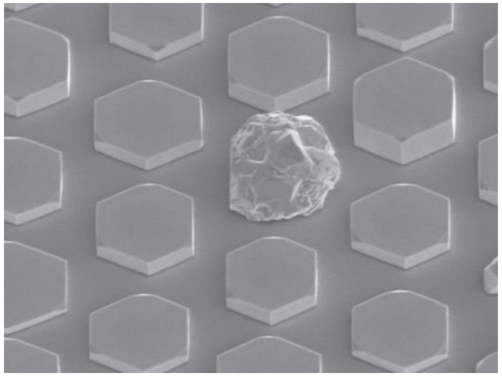


Kunert et al, APL 109, 091101 (2016)

- RT electroluminescence of InGaAs *pin* on Si (University of Tokyo)



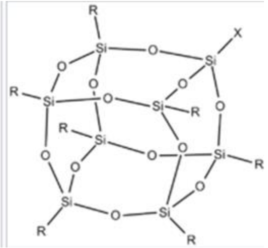
Kjellman et al, APL104, 241103 (2014)



SAG for III-V planar MOSFET with ultra-short gate

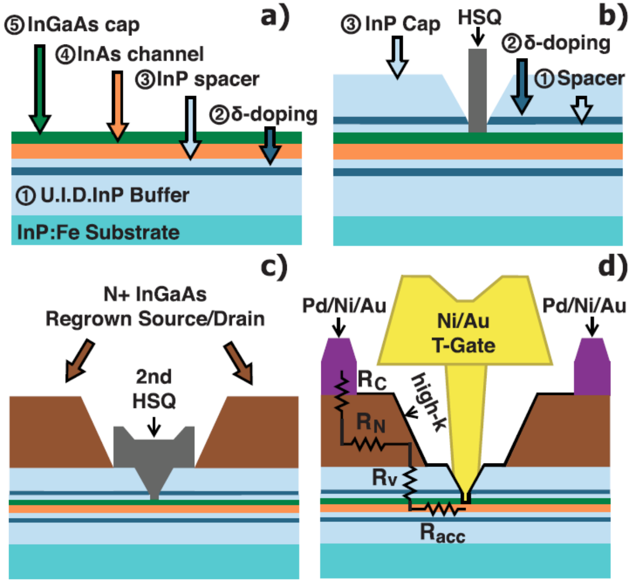
SAG for III-V MOSFET with ultra-short gate

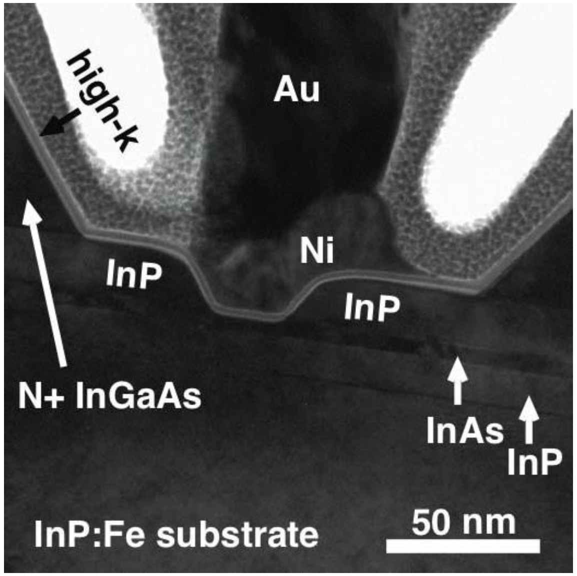
Process using HSQ dummy gate



HSQ = hydrogen silesquioxane = inorganic compounds ($H_8Si_8O_{12}$)
Can be deposited by spin-coating and cross-linked with e-beam or EUV radiation
Pattern width down to 10 nm achievable

- Fabrication of InGaAs MOSFET on InP with 30 nm gate length (UCSB)





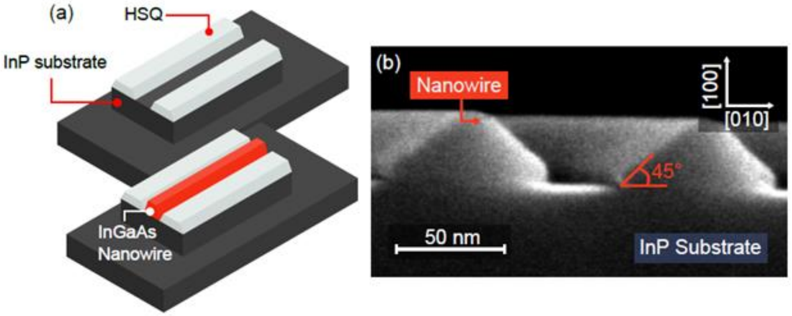
Double step MOCVD regrowth => optimization of the gate stack to achieve f_t=420 GHz

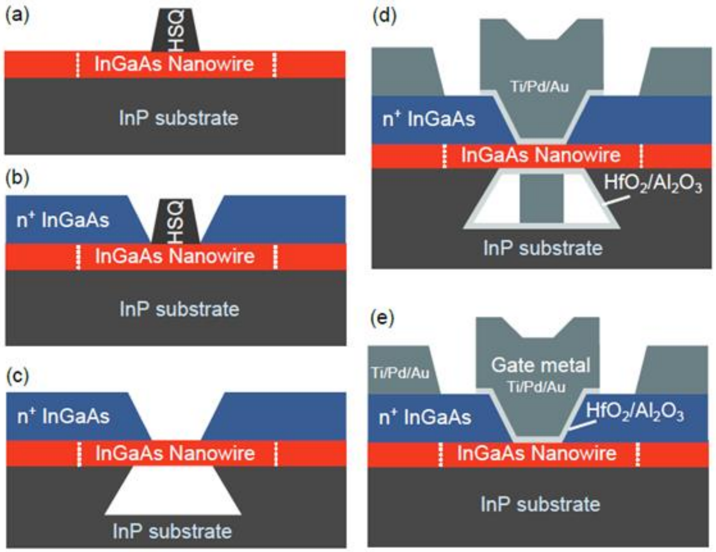
Wu et al, EDL IEEE EDL 39, p. 472 (2018)

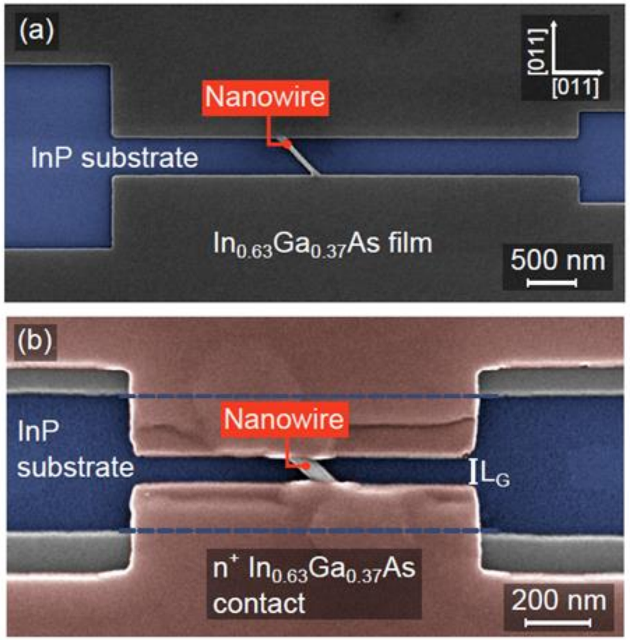
SAG for III-V MOSFET with ultra-short gate

Process using HSQ dummy gate

- Fabrication of single suspended InGaAs NW MOSFET on InP (Lund University)







Zota et al, IEDM 2016

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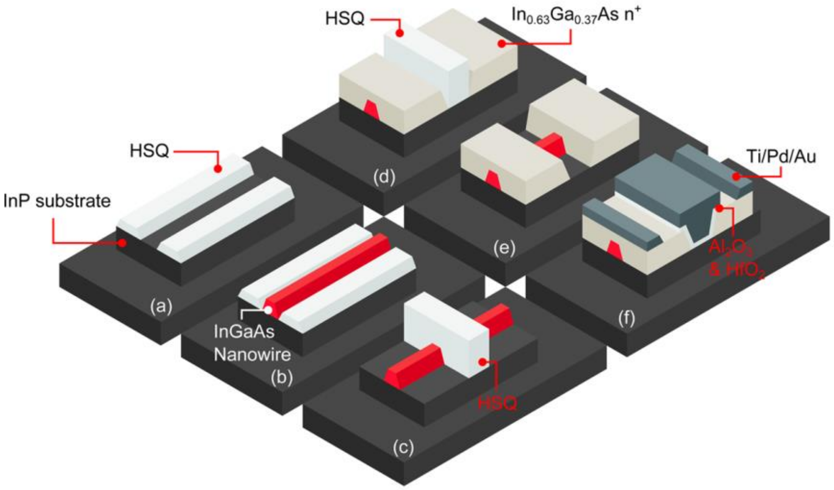
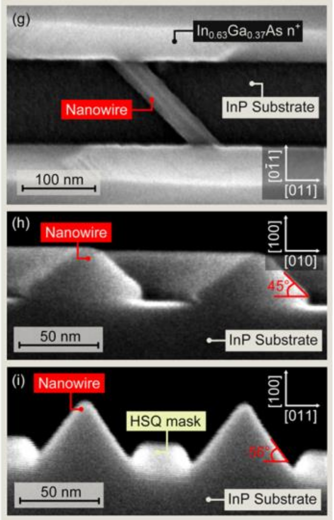
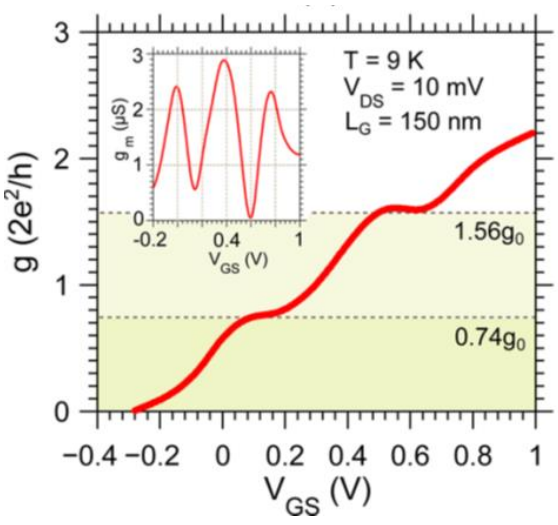
SAG for ballistic nano-devices

- Observation of quantum conductance plateaus in InGaAs nanowire grown using HSQ process

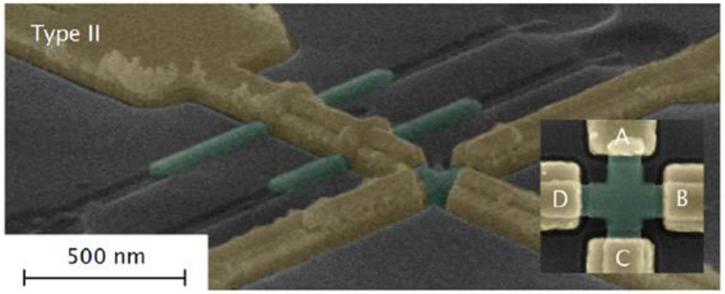


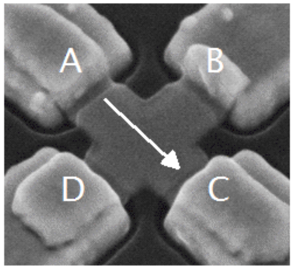


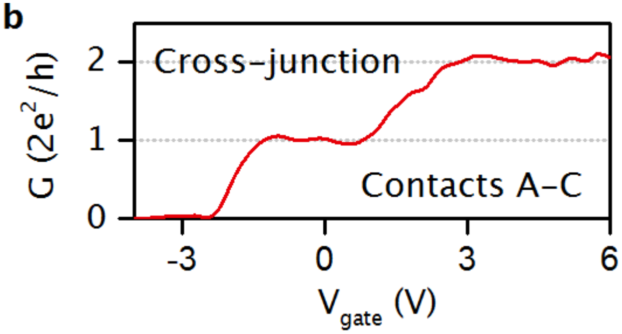


Zota et al, ACS Nano 9, p. 9892 (2015)

- Observation of quantum conductance plateaus in InAs NW and cross-junction using TASE







Gooth et al, Nano Lett. 2017, 17, 2596−2602
Gooth et al, Appl. Phys. Lett. 110, 083105 (2017)

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Outline

- Selective Area Growth: definition, motivation and method?

- Opportunities for Selective Area Growth (SAG) for III-V nanostructures
  - Optoelectronics
  - III-V MOSFET development
  - Quantum technologies

- Review of SAG developments (mainly MOCVD)

- Development of MBE-SAG for in-plane III-V nanostructures
  - Mask preparation
  - Surface deoxidation
  - Growth conditions
  - Atomic H assisted MBE
  - Examples of III-V nano-SAG using MBE

- Conclusion and prospects

What about SAG with MBE?

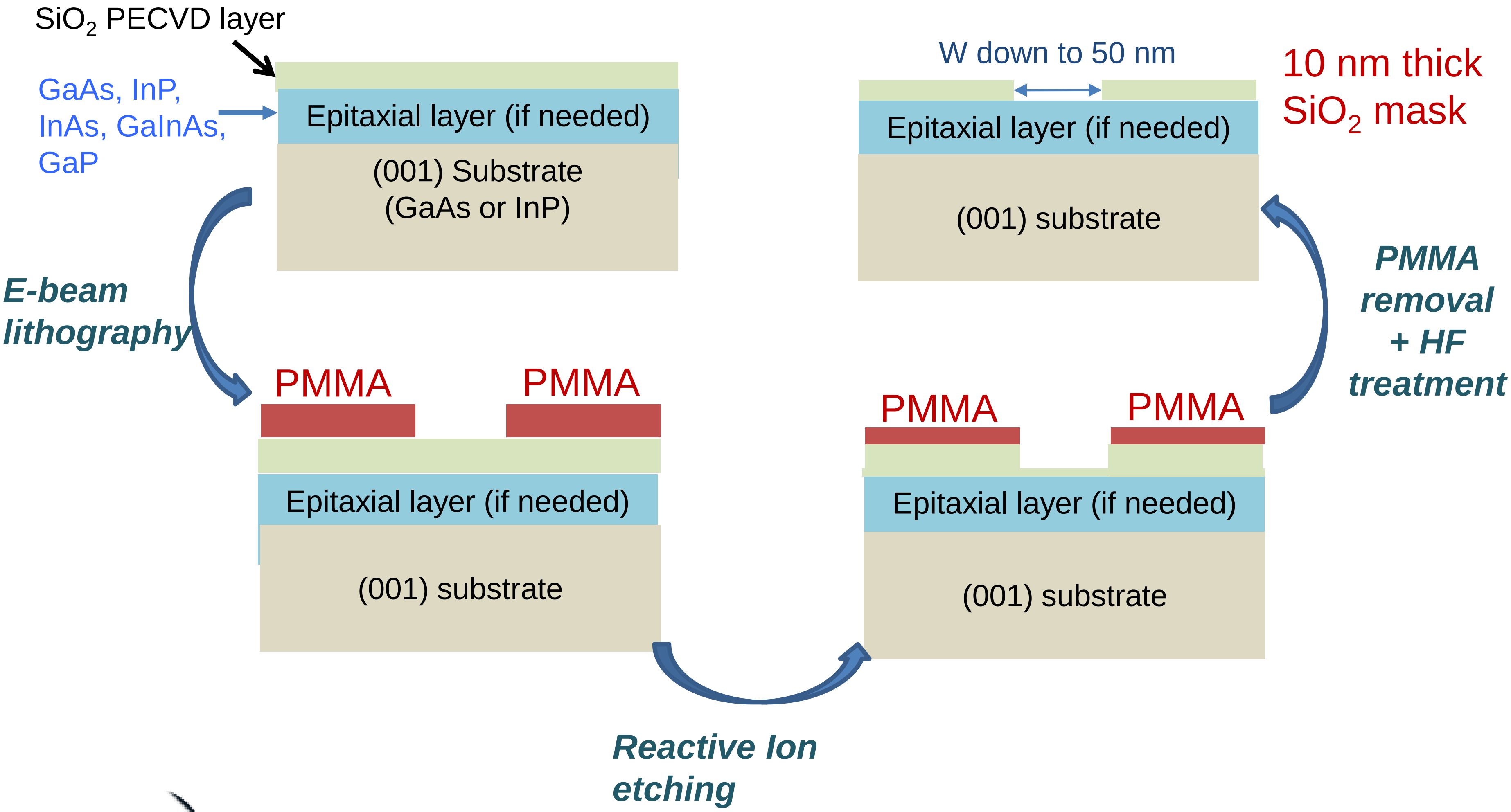
- Low thermal budget compared to MOCVD (lower growth temperature)
- Higher active doping density at low temperature
- Possibility of in-situ supraconductor deposition (ex: Al)

<u>Challenges</u>:

- Surface cleaning and deoxidation before regrowth
- Find growth conditions for selectivity:
  temperature, growth rate, V/III ratio

Our mask preparation for SA-MBE

Process for large area mask with small aperture



SiO_2 PECVD layer

GaAs, InP, InAs, GaInAs, GaP

Epitaxial layer (if needed)

(001) Substrate (GaAs or InP)

E-beam lithography

PMMA

PMMA

Epitaxial layer (if needed)

(001) substrate

Reactive Ion etching

PMMA

PMMA

Epitaxial layer (if needed)

(001) substrate

PMMA removal + HF treatment

W down to 50 nm

10 nm thick SiO_2 mask

Epitaxial layer (if needed)

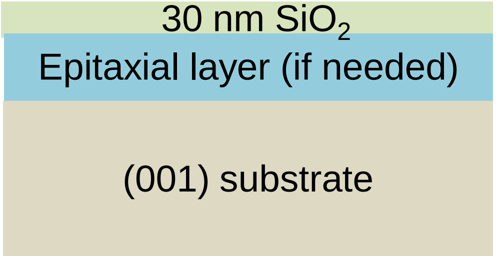
(001) substrate

Mask preparation for SA-MBE

Process for large area mask with small aperture

Plasma Enhanced Chemical Vapor deposition
Oxford Plasmalab 80+ chamber

- Sample heated at 300 ºC under vacuum
- N_2 purge
- RF Plasma with SiH_4 and N_2O
- Ex-situ thickness control

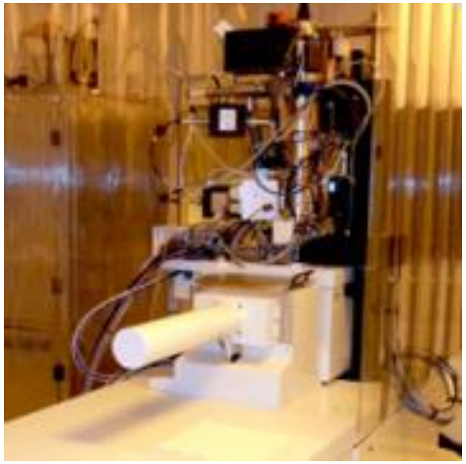


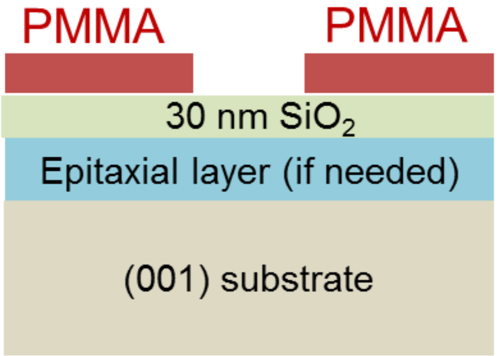
Mask preparation for SA-MBE

Process for large area mask with small aperture

E-beam lithography
EBPG 5000plus (100kV)

- Spin coating PMMA (thickness 100 nm)
- E-beam exposure
- Development with MIBK/IPA
- Pattern width down to 50 nm achieved





PMMA PMMA

30 nm SiO_2

Epitaxial layer (if needed)

(001) substrate

Mask preparation for SA-MBE

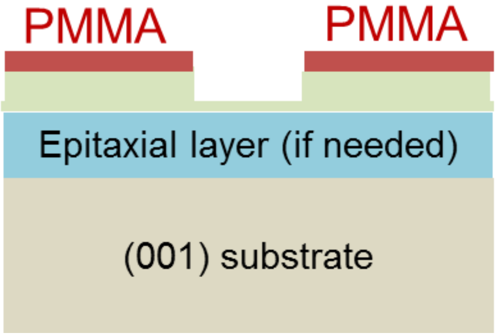
Process for large area mask with small aperture

Reactive Ion Etching
Oxford Plasmalab 80+ chamber

- Short O_2 plasma etching to remove PMMA residues in openings

- CHF3/CF4/Ar plasma etching

- Etching depth ≈ 15-20 nm (SiO_2 not fully opened)



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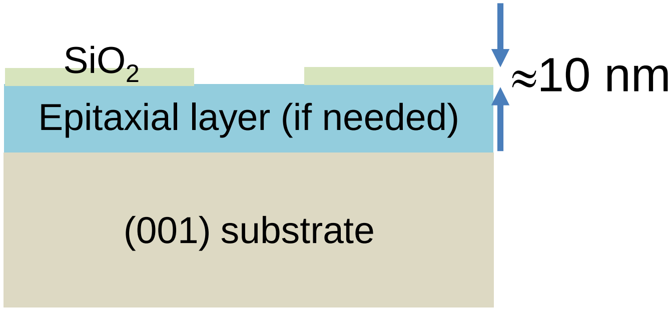
Mask preparation for SA-MBE

Process for large area mask with small aperture

SiO_2 opening before growth

- Dilute HydroFluoric acid
  ☹ Be careful if the top surface is GaSb (etched by HF!)

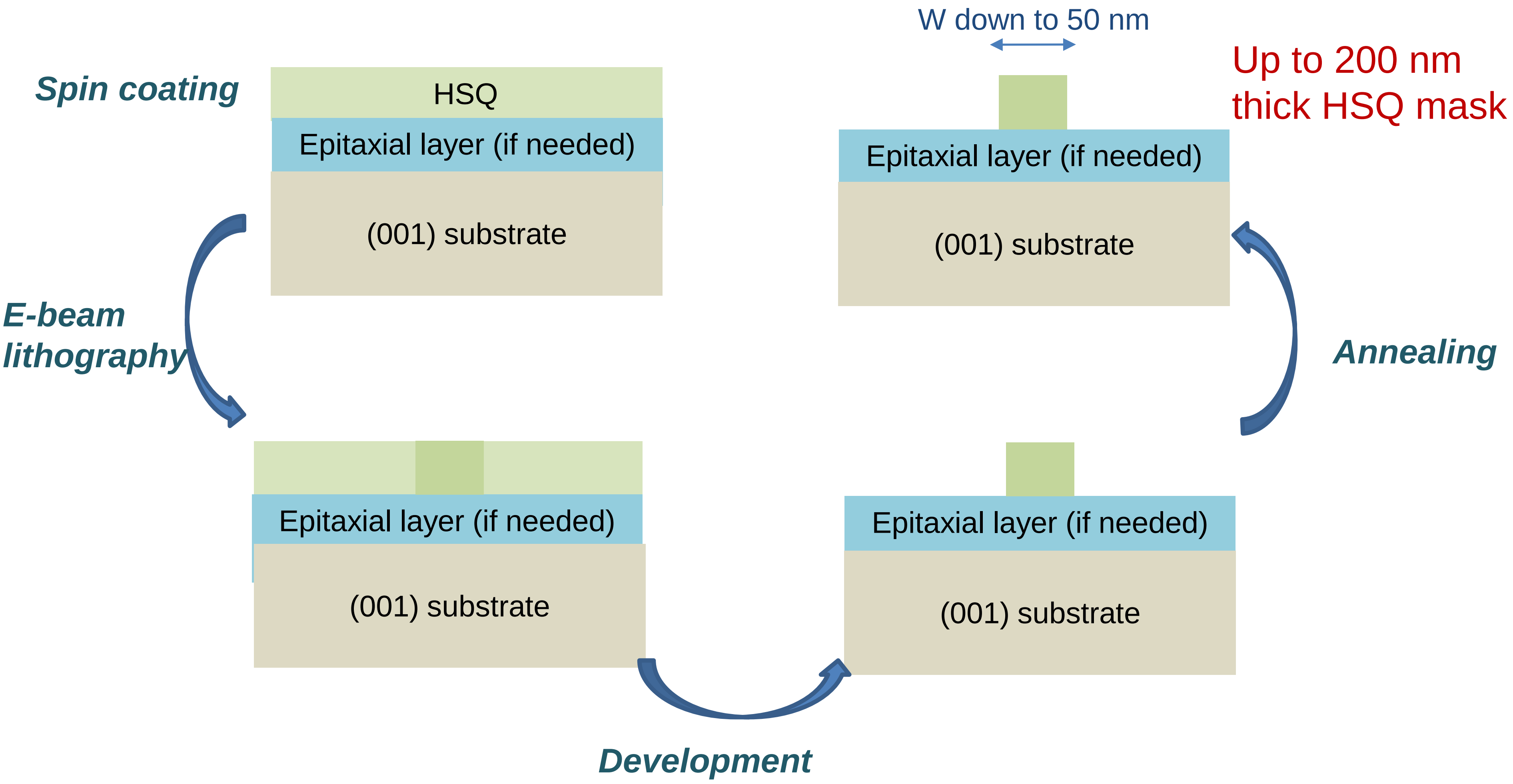
- Final thickness of the mask ≈ 10 nm



Sample is then introduced rapidly in MBE outgasing chamber for 200° C annealing before growth

Mask preparation for SA-MBE

Process for small area mask (HSQ process)



Spin coating

HSQ

Epitaxial layer (if needed)

(001) substrate

E-beam lithography

Epitaxial layer (if needed)

(001) substrate

Development

Epitaxial layer (if needed)

(001) substrate

Annealing

W down to 50 nm

Up to 200 nm thick HSQ mask

Epitaxial layer (if needed)

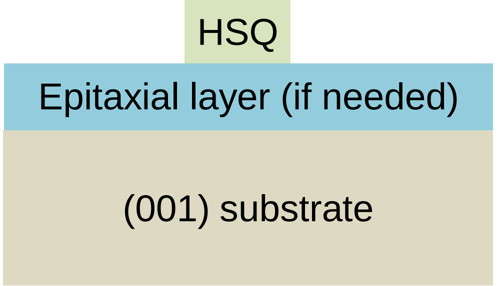
(001) substrate

Mask preparation for SA-MBE

Process for small area mask (HSQ process)

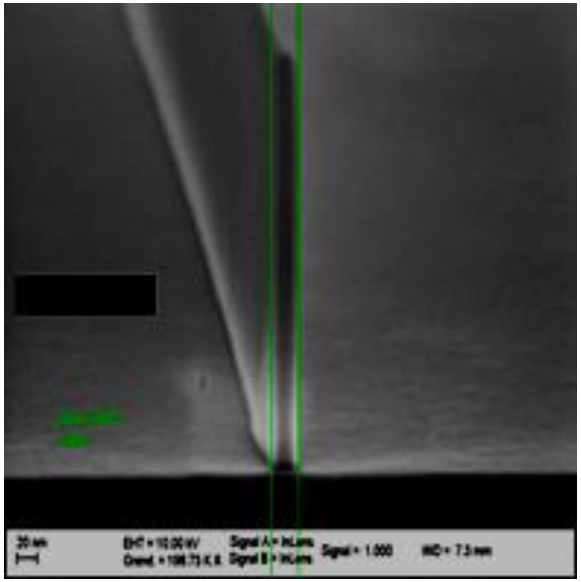
E-beam cross-linking + Development

- E-beam exposure (100 kV)
- Development:
- 300° C annealing for densification


HSQ

Epitaxial layer (if needed)

(001) substrate



Width of 25 nm for a height of 200 nm can be achieved on InP substrate

M.Pastorek, PhD thesis (IEMN, 2017)

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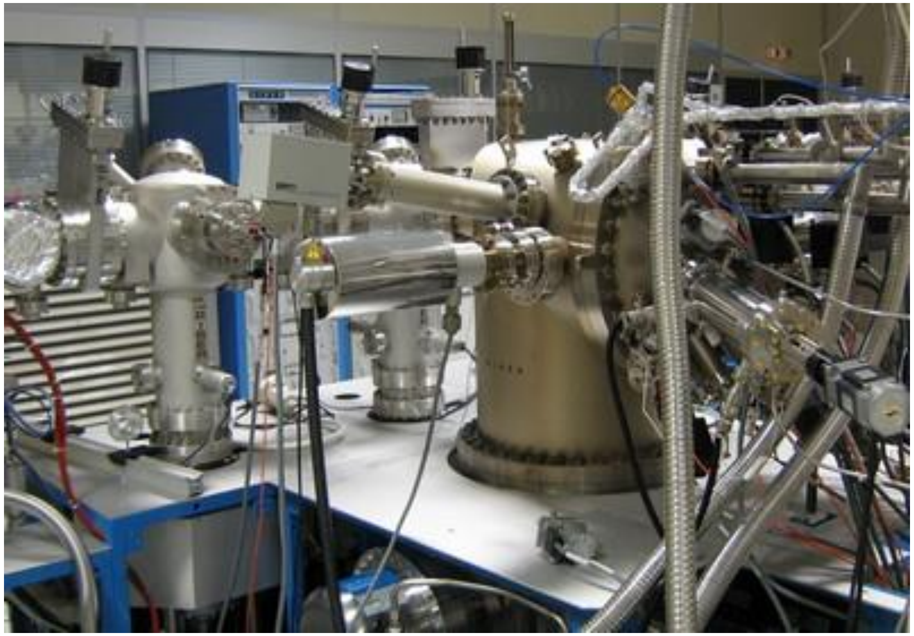
IEMN MBE systems

Riber Compact 21 TM

As valved cracker (Riber VAC 500)
Sb valved cracker (Veeco RB 200)
Ga, In, Al
Si, Te
CBr_4 gas injector for C doping
RF plasma cell for atomic H flux

Riber 32P



AsH_3 and PH_3 gas injector
Sb valved cracker (Veeco RB 200)
Ga, In, Al
Si, Be
CBr_4 gas injector for C doping

UHV connected systems + connection with ESCA for surface analysis

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Surface preparation for SA-MBE

How minimizing surface roughness and carbon contamination whithout any buffer ?

- GaAs surface deoxidization before regrowth

Comparison of 3 different preparations:

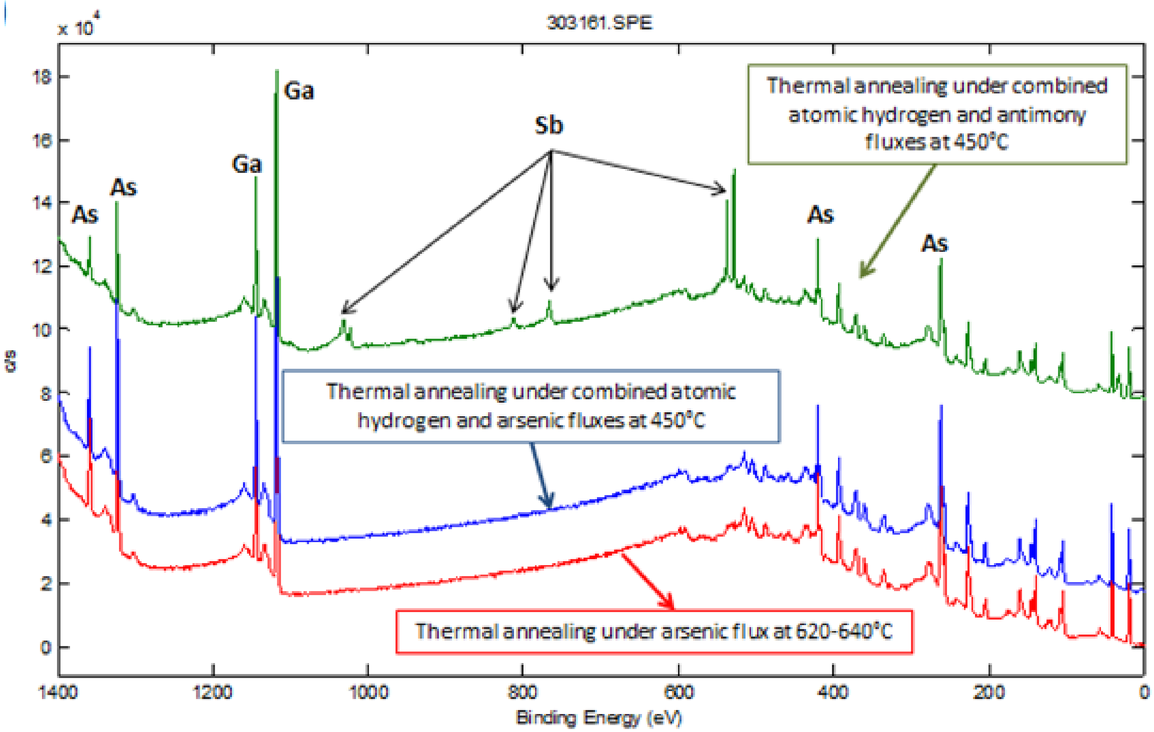
- « Classical » thermal deoxydization under As_4 flux up to 620° C
- Deoxydization under As_4 + H atomic flux up to 450° C
- Deoxydization under Sb_2 flux + H atomic flux up to 450° C

RF power = 400 W
H_2 =3 sccm

Surface preparation for SA-MBE

GaAs surface analysis

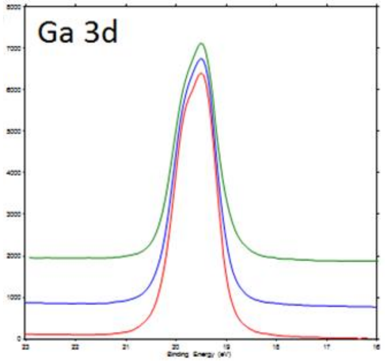
- GaAs surface deoxidization before regrowth: surface analysis with XPS

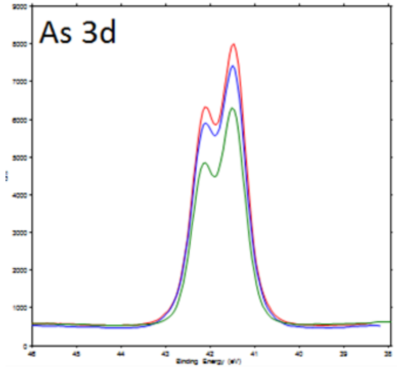


Thermal annealing under combined atomic hydrogen and antimony fluxes at 450°C

Thermal annealing under combined atomic hydrogen and arsenic fluxes at 450°C

Thermal annealing under arsenic flux at 620-640°C





Deoxidization complete on the 3 samples, no carbon detectable

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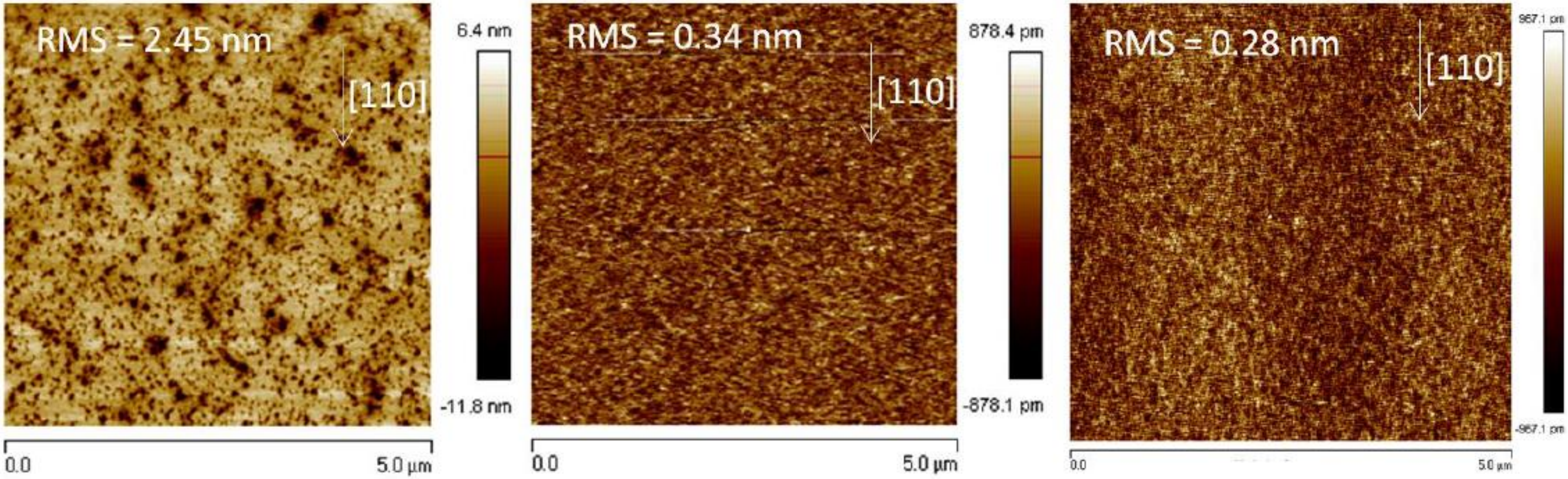
Surface preparation for SA-MBE

GaAs surface analysis

- GaAs surface deoxidization before regrowth: roughness analysis



(a) Thermal annealing under arsenic flux at 620-640°C

(b) Thermal annealing under combined atomic hydrogen and arsenic fluxes at 450°C

(c) Thermal annealing under combined atomic hydrogen and antimony fluxes at 450°C

Reduced roughness for sampes deoxidized at 450° C under H atomic flux

Surface preparation for SA-MBE

InP surface preparation

- Different InP surface preparation before InGaAs/InP QW epitaxy:

InP buffer (70 nm)
$In_{0,53}Ga_{0,47}As$ (30 nm)
InP buffer (300 nm)
InP SI substrate

Reference
(deoxidized under P2 flux @ 520° C)

InP buffer (70 nm)
$In_{0,53}Ga_{0,47}As$ (30 nm)
No buffer
InP SI substrate

(deoxidized under P2 flux @ 520° C)

InP buffer (70 nm)
$In_{0,53}Ga_{0,47}As$ (30 nm)
No buffer
InP SI substrate

(deoxidized under As_4 flux @ 520° C)

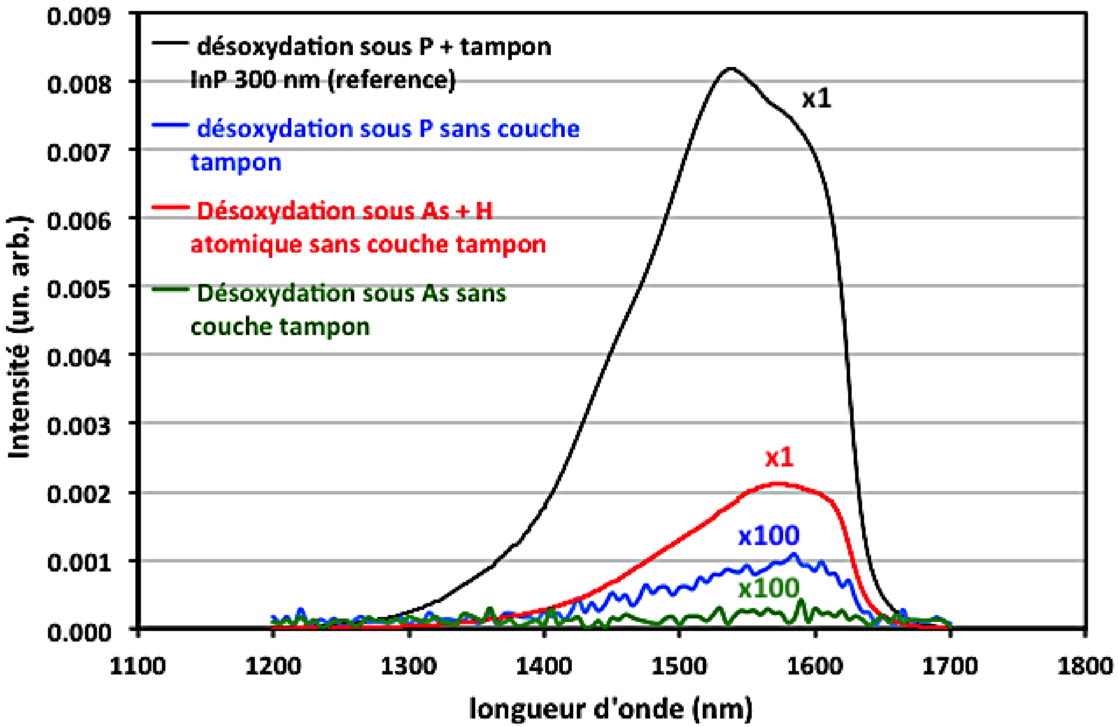
InP buffer (70 nm)
$In_{0,53}Ga_{0,47}As$ (30 nm)
No buffer
InP SI substrate

(deoxidized under As_4 flux + atomic H @ 480° C)

Surface preparation for SA-MBE

InP surface preparation

- 300K Photoluminescence of InGaAs/InP QW



2 to 3 order of magnitude lower PL intensity than reference sample for buffer free epitaxy…
…except for the one with atomic H flux during deoxidation (same order of magnitude)

Probably reduced carbon incorporation in InGaAs QW using atomic H flux

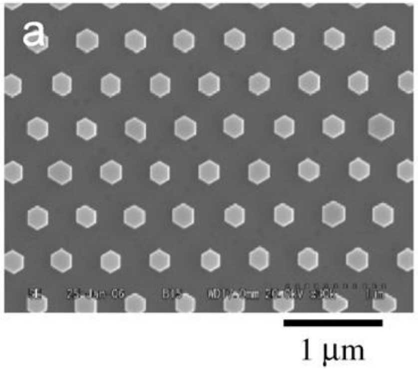
Growth conditions for SA-MBE

Homoepitaxy

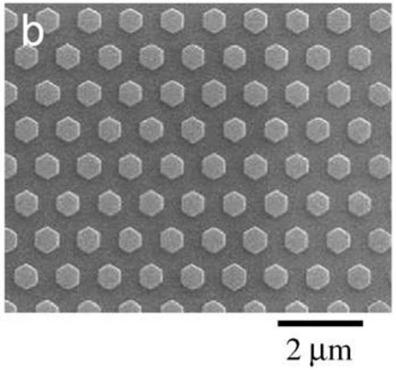
Growth conditions for SA-MBE

GaAs homoepitaxy

- GaAs nanopillars on (111) GaAs substrate



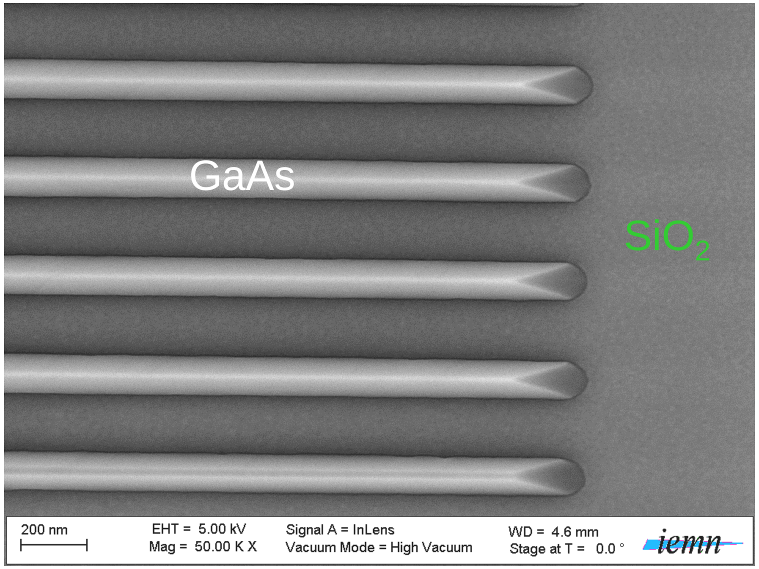
AlGaAs native oxyde mask



SiO_2 mask

Yoshiba et al, JCG301–302 (2007) 190

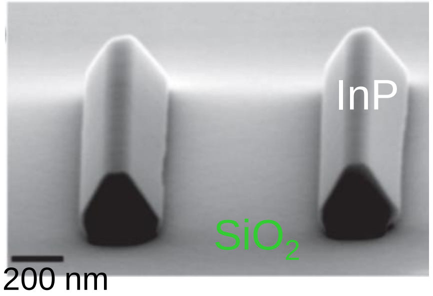
- In-plane GaAs nanowires on (001) GaAs



*Growth temperature = 595° C (**580° C< T_G< 620° C**)*
Growth rate= 0,1 ML.s^{-1}

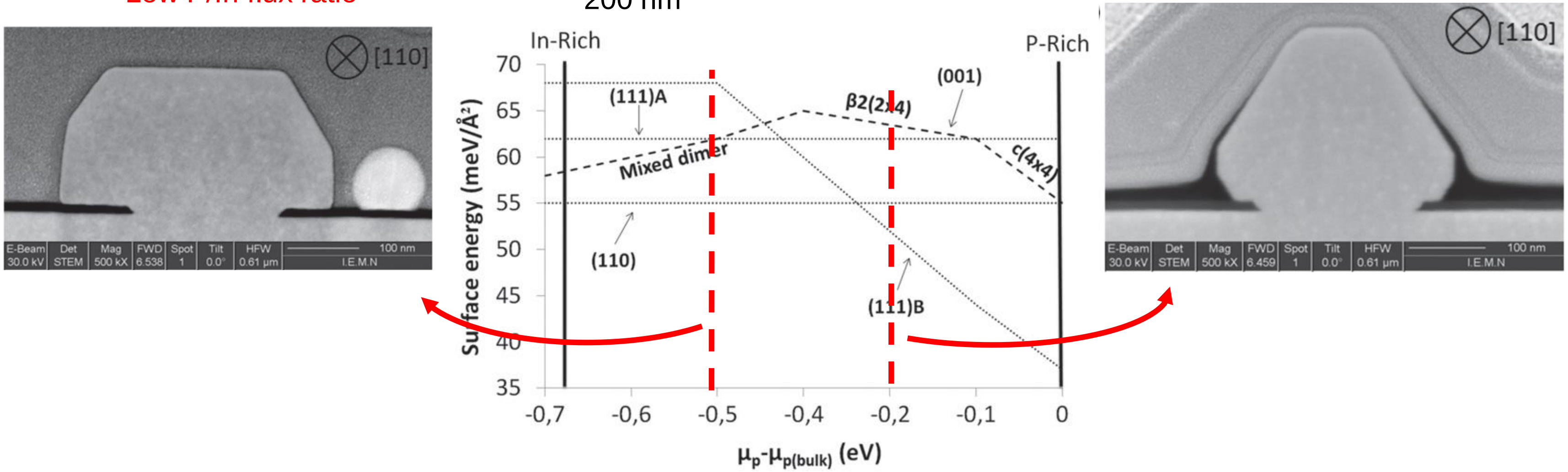
Growth conditions for SA-MBE

InP homoepitaxy



Low P/In flux ratio

High P/In flux ratio



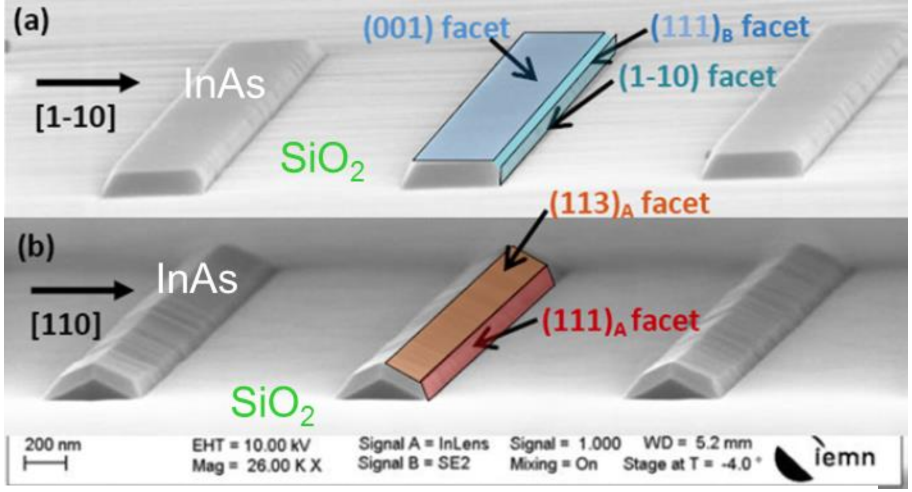
⇨ Possibility to control the shape of the nanostructure playing with V/III ratio

M.Fahed et al, Nanotechnology 26 (2015) 295301

Growth conditions for SA-MBE

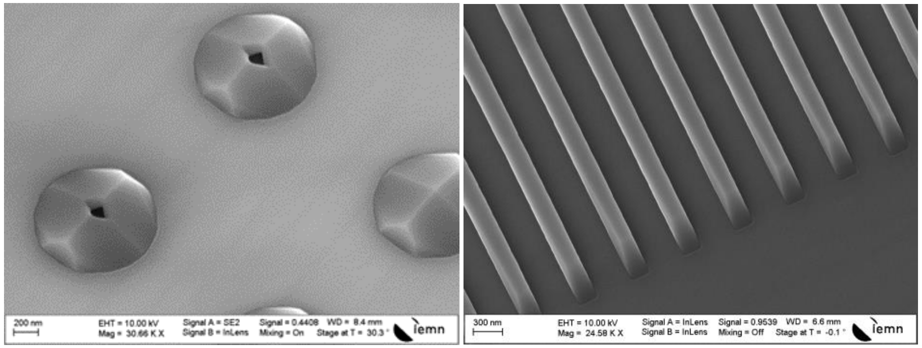
InAs homoepitaxy

- In-plane InAs nanostructures on InAs

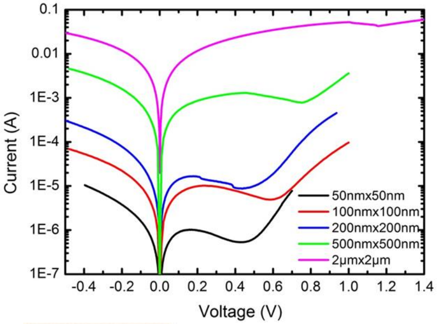


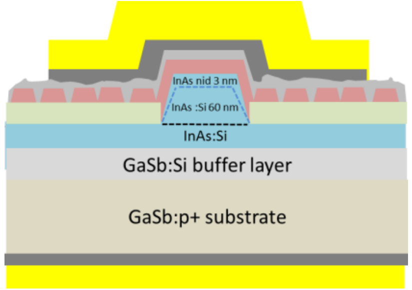
*Growth temperature = 500° C (**470° C< T_G< 510° C**)*

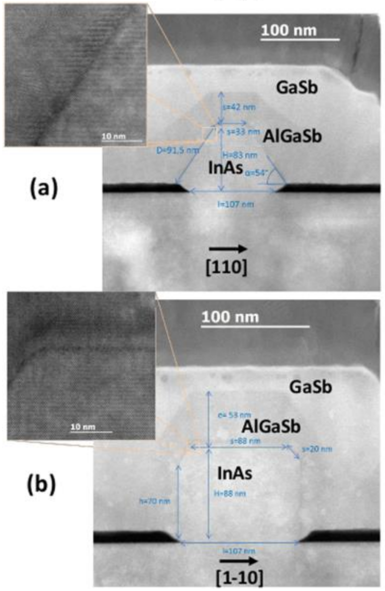
Growth rate= 0,2 ML.s^{-1}

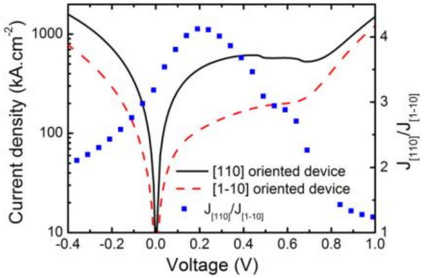


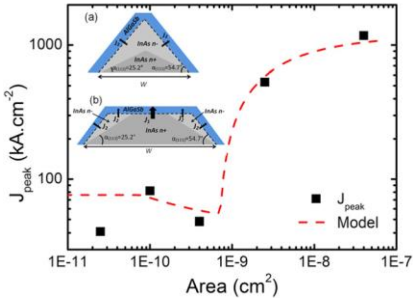
- InAs/AlGaSb core-shell tunnel diodes











L.Desplanque et al, Nanotechnology 25,46 (2014) 465302

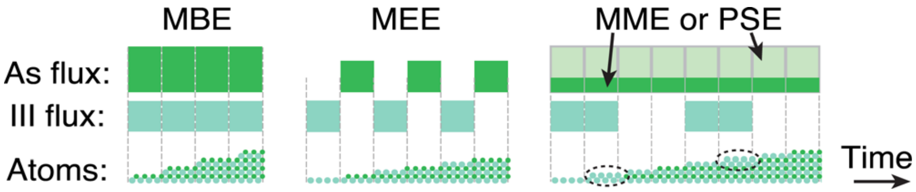
On (001) substrate, strong impact of stripe orientation on faceting!

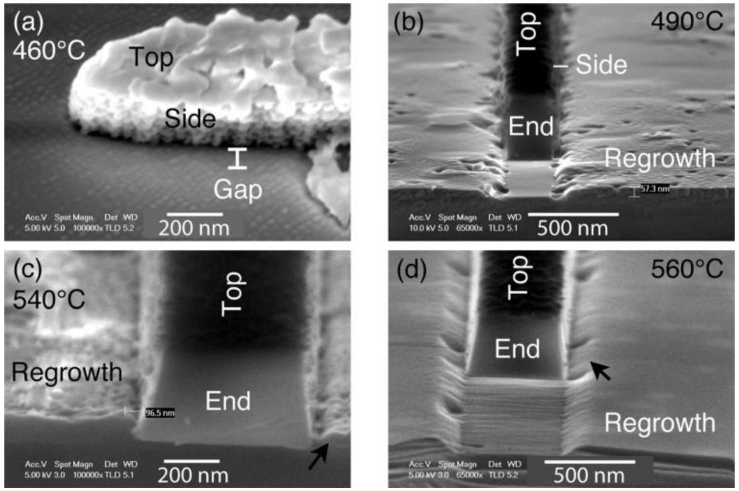
Growth conditions for SA-MBE

How to reach selectivity for InGaAs?

Metal modulated epitaxy (MME)

InGaAs selective MBE growth with HSQ mask

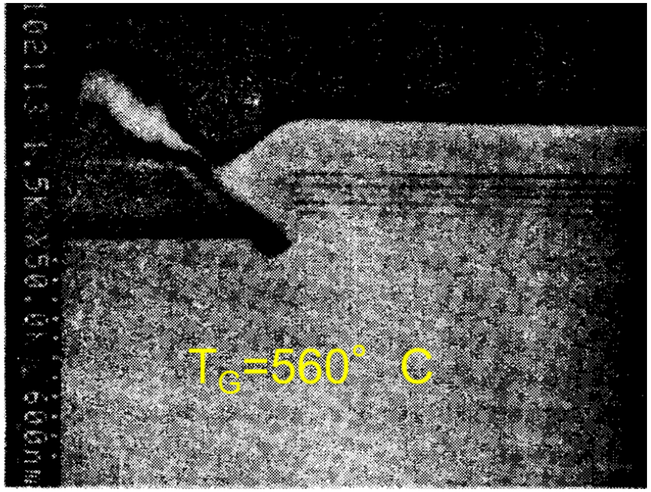




M.A.Wistey et al, JVST B 33 p011208 (2015)

Atomic H assisted MBE ?

Selective growth of InGaAs/InP layers by GS-MBE using H atomic irradiation

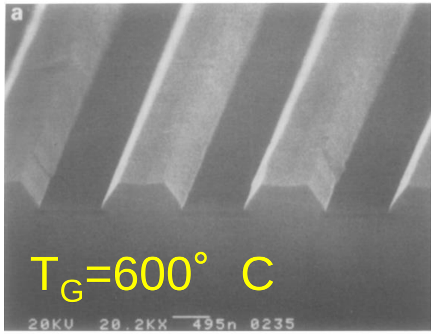


Kuroda et al, IEEE IPRM (1993)

Growth conditions for SA-MBE

Atomic hydrogen-assisted MBE growth

Selective area growth of GaAs by ECR-MBE



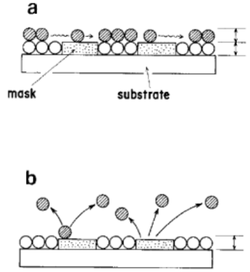
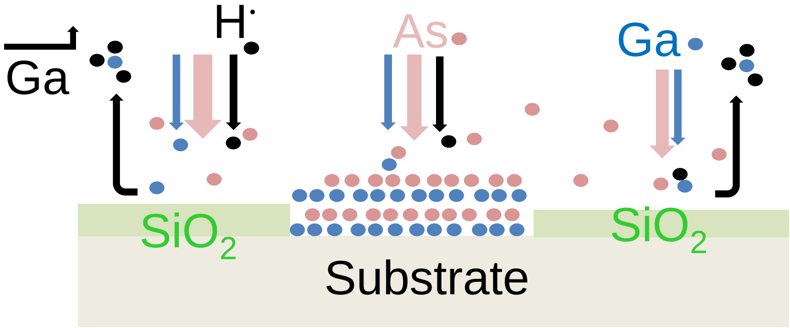


Fig. 3. Schematic diagram to explain the mechanism in the selective area growth by ECR-MBE: (a) migration process and (b) desorption process. The open and closed circles show the impinging atoms to the unmasked GaAs surface and those to the Si_3N_4 mask surface, respectively.

Yamamoto et al, JCG 93 p705 (1989)



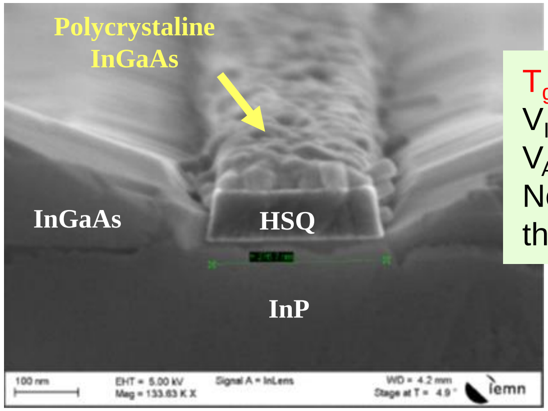
Atomic H flux during the growth reduces Ga nucleation on the SiO_2 mask: same mechanism than for GaO_x removal?

⇨ the growth selectivity can be obtained at lower temperature

Growth conditions for SA-MBE

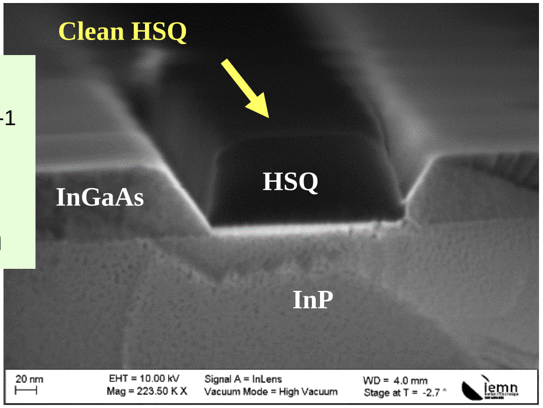
Atomic H-assisted MBE growth of InGaAs

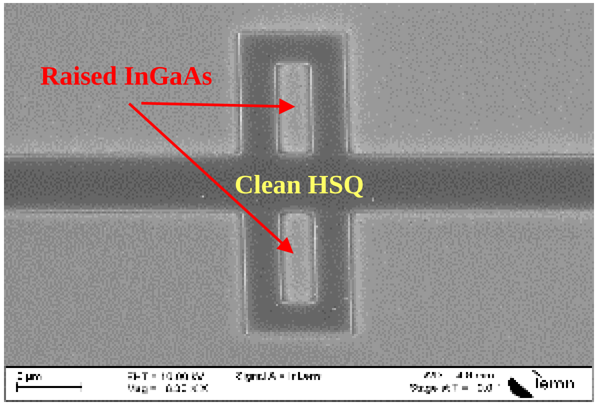
With no atomic H during growth



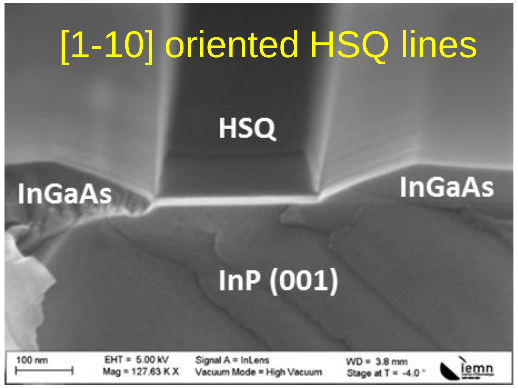
T_{growth}=490° C
V_{InGaAs}~ 0.2ML.s^{-1}
V_{As}=1 ML.s^{-1}
Nominal thickness=50 nm

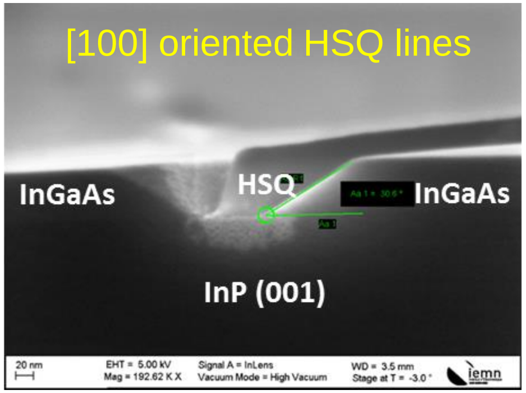
With atomic H during growth

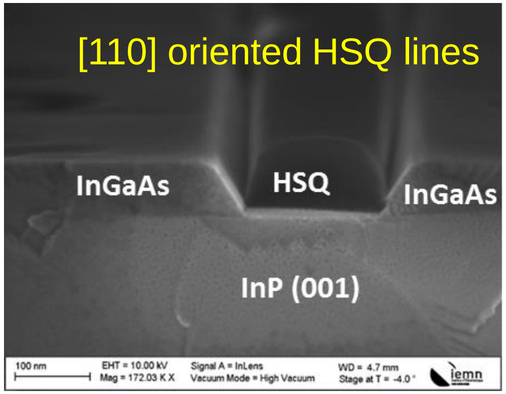


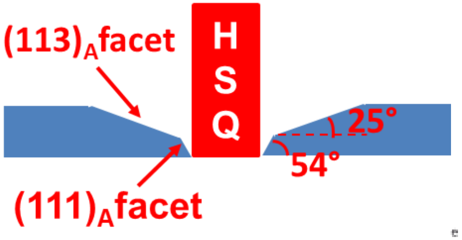


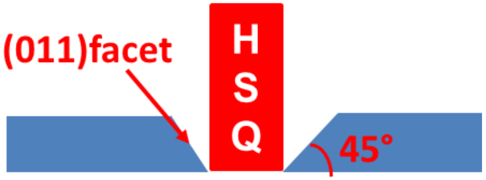
low growth rate (0.2 ML.s^{-1}) + H atomic hydrogen ⇨ InGaAs MBE selective growth down to **490° C**

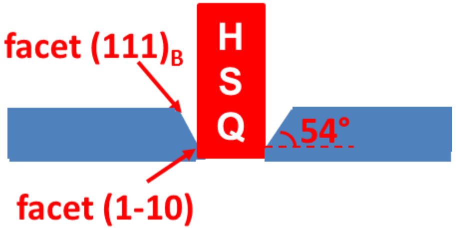










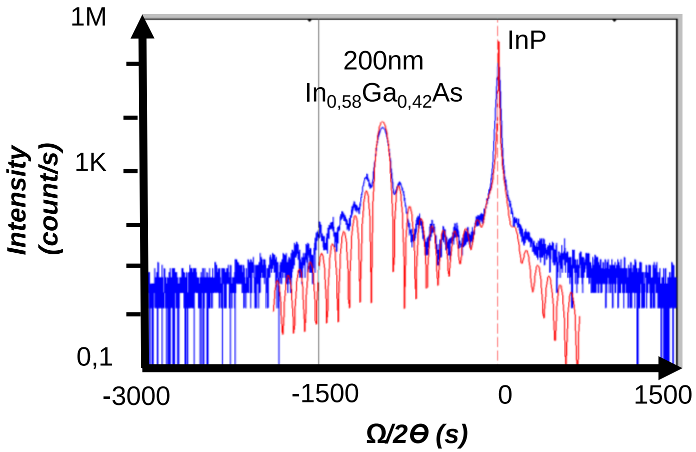


Growth conditions for SA-MBE

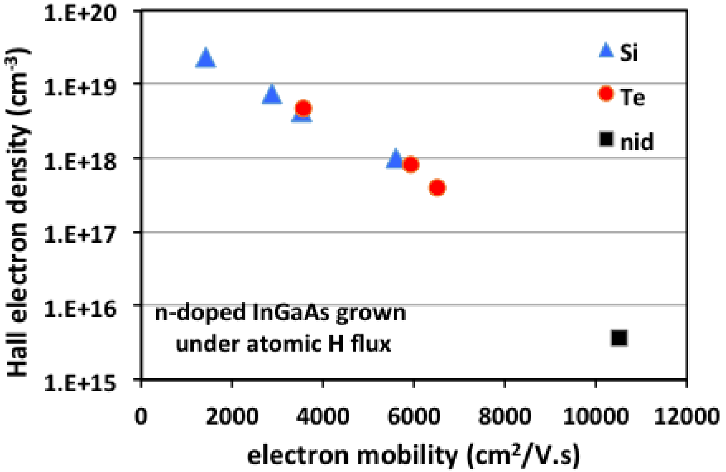
Atomic H-assisted MBE growth of InGaAs

- Impact of atomic H on InGaAs properties ?

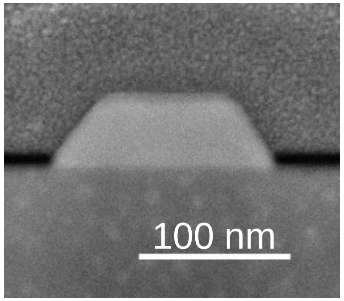
Structural quality (2D layer)

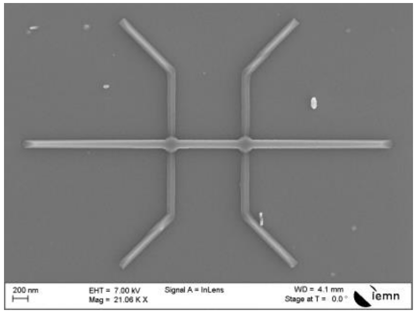


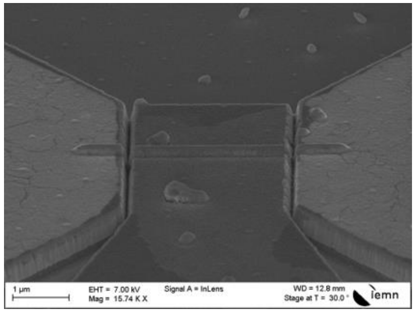
Doping (2D layer)



Electrical properties of InGaAs nanostructures
(see poster A.Bucamp)







Growth conditions for SA-MBE

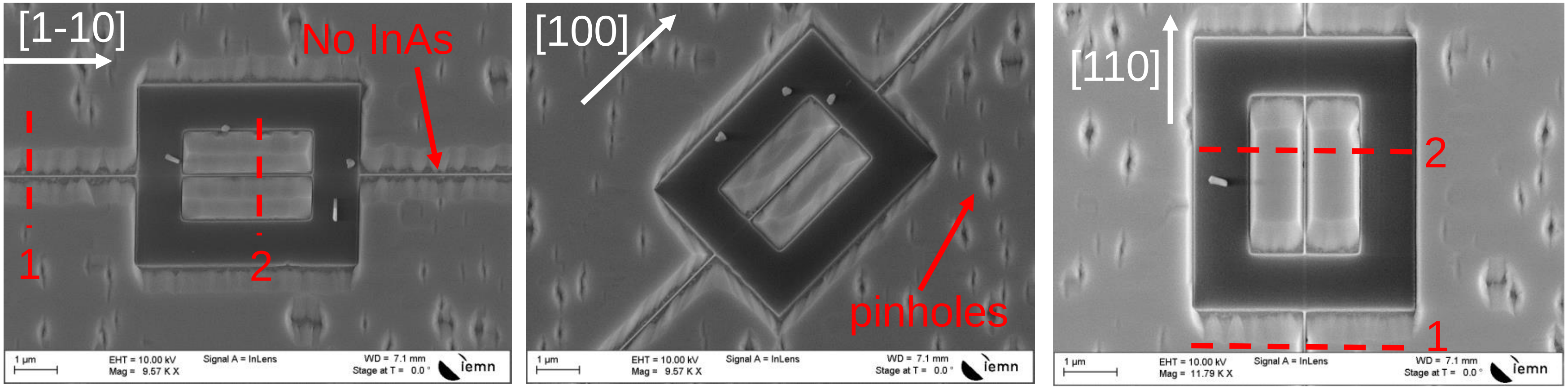
Lattice mismatched materials

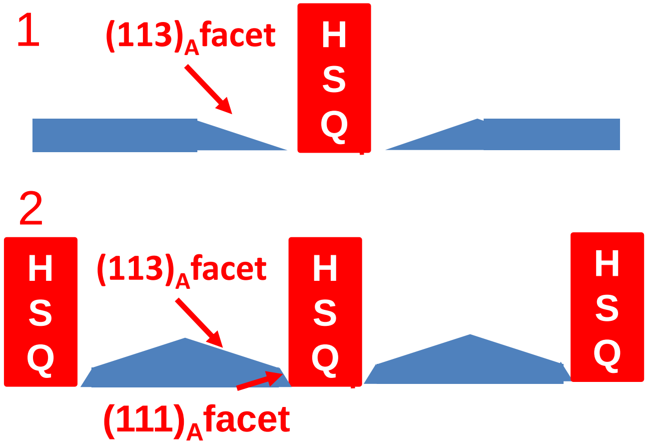
Growth conditions for SA-MBE

InAs on InP

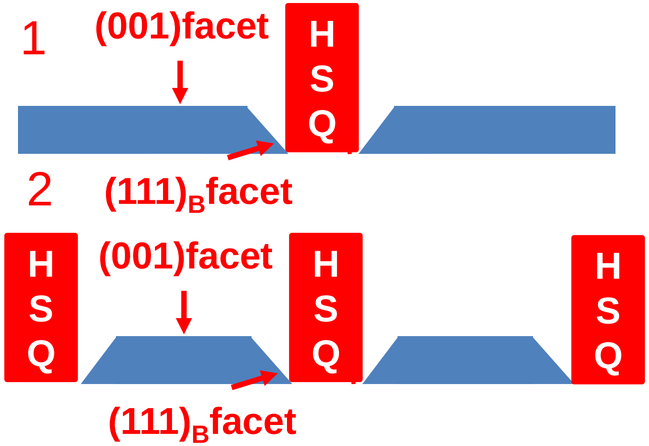
150 nm InAs:Si (10^{19} cm^{-3}) on QW layer @ **450° C** under atomic Hydrogen, V_{growth}=0.2 ML.s-1, As/In=5

Strain induced InAs 3D growth mode





- ⇨ Pinholes are still visible on large area
- ⇨ No pinholes in µm scaled area
- ⇨ Small angle facets result in edge roughness
- ⇨ Reduced roughness in confined area (formation of larger angle facets)



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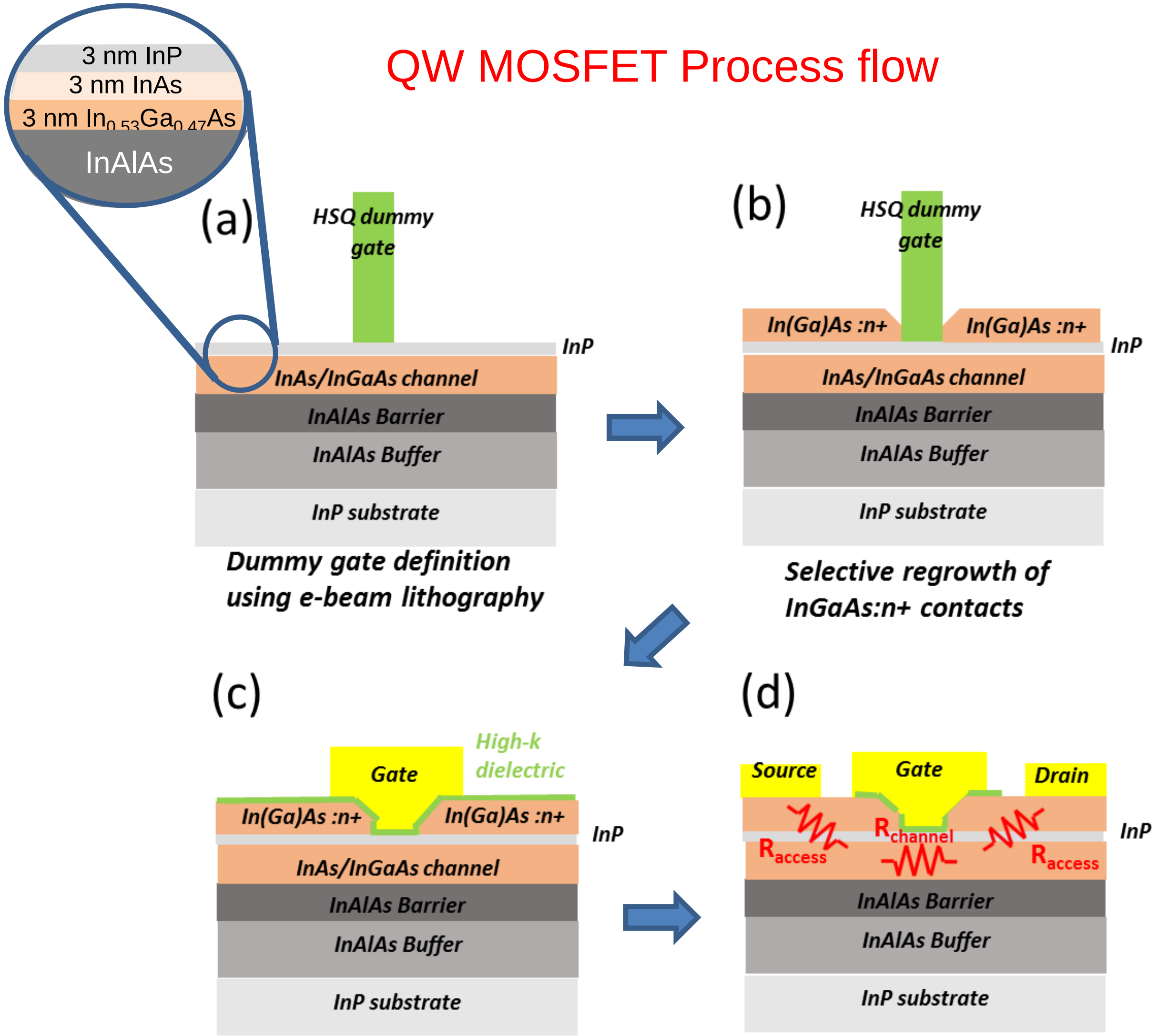
Raised InGaAs:n+ Source and Drain for QW MOSFET

QW MOSFET Process flow



Dummy gate definition using e-beam lithography

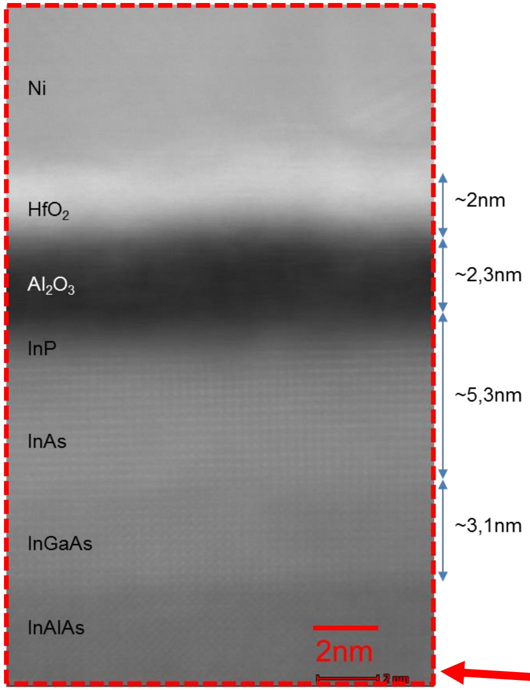
Selective regrowth of InGaAs:n+ contacts

Gate oxide deposition by ALD + Gate deposition

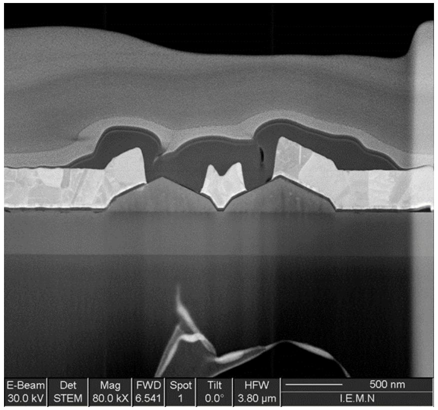
Oxide opening + source and drain metal deposition

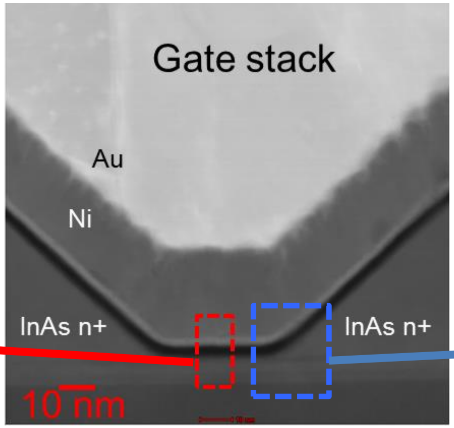
Growth conditions for SA-MBE

InAs:n+ raised source-drain contacts for QW MOSFET on InP

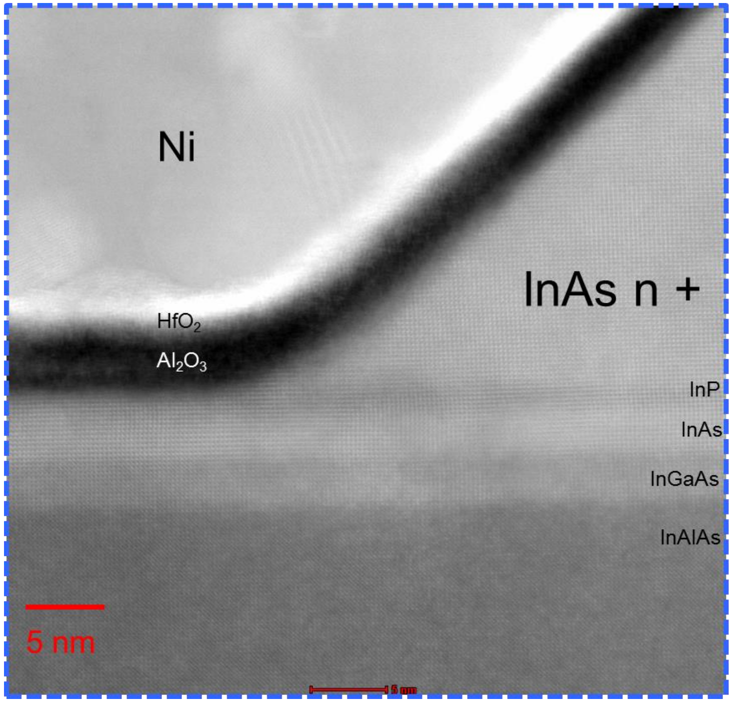


Channel





TEM analysis from A.Addad (UMET)



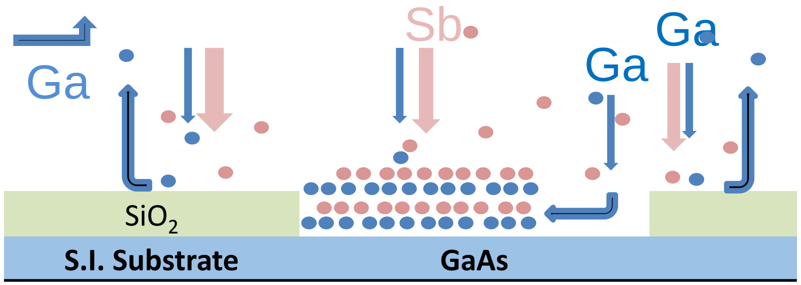
Contact area

⇨ Improvement of the access resistances using InAs rather than InGaAs (reduced R $_{\text{metal/SC}}$)

M.Pastorek, PhD Thesis IEMN (2017)

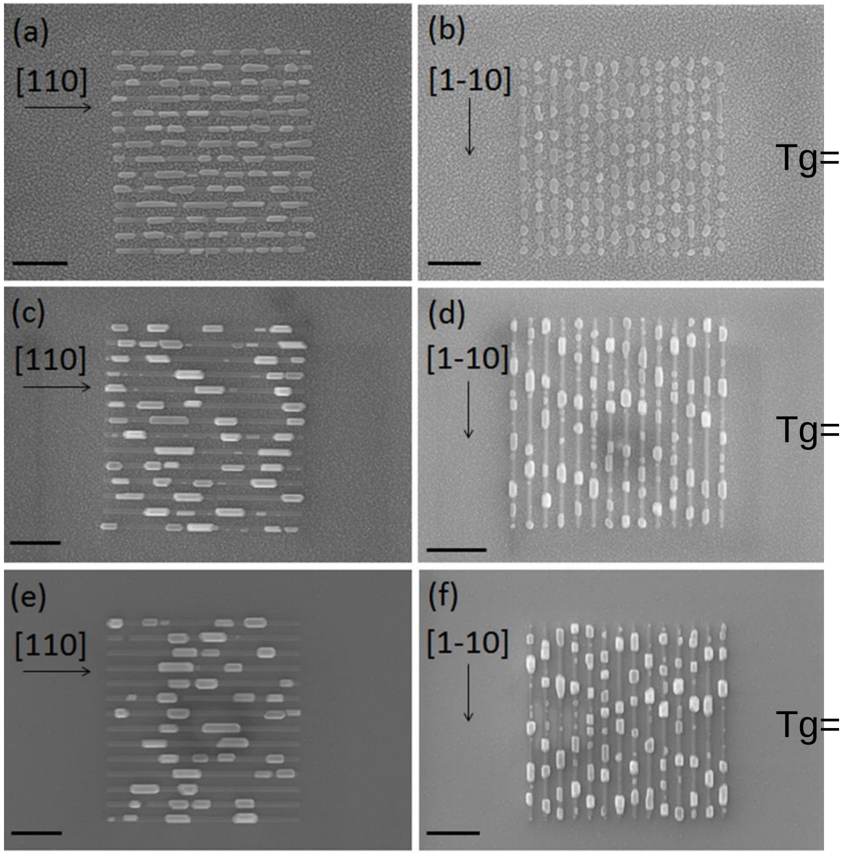
Growth conditions for SA-MBE

GaSb on GaAs



<u>Growth conditions</u>:

- *Thermal annealing to 620° C under As$_4$ for GaAs deoxidation*
- *Deposition of 25 nm (nominal thickness) of GaAs @ 590° C to smooth the surface after deoxidation*
- *Deposition of 20 nm (nominal thickness) of GaSb with low growth rate and various Tg*
- *No H atomic flux during growth*



Tg=470° C

Tg=510° C

Tg=540° C

➢ Need to get selectivity at low temperature to fill the aperture !

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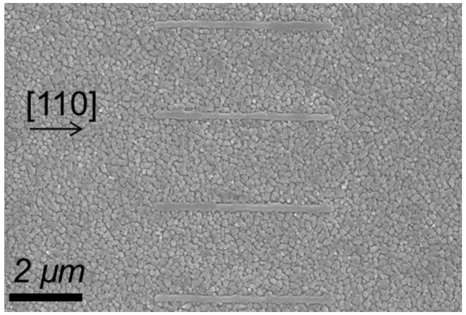
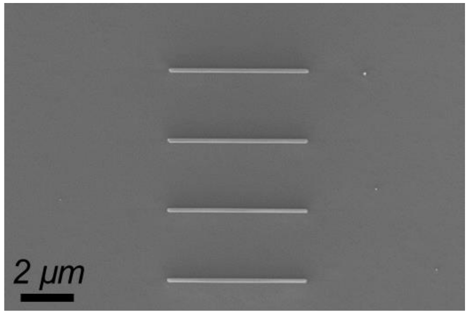
Growth conditions for SA-MBE

GaSb on GaAs

65 nm GaSb inside 100 nm wide apertures; ***T_g=470° C****; Sb/Ga=10; V_{Ga}=0,1 ML.s^{-1}*



Without atomic hydrogen



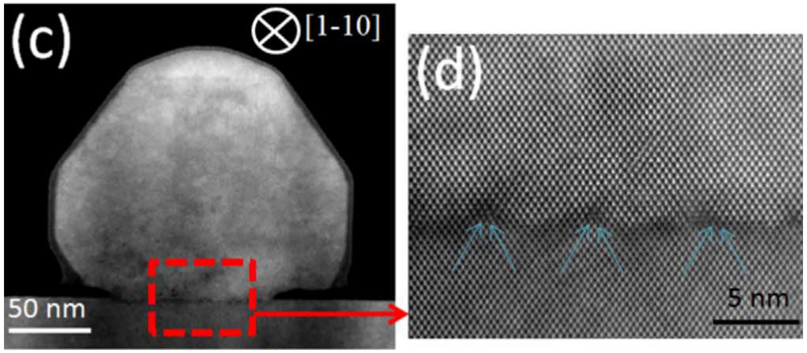
With atomic hydrogen

Seletive growth of GaSb on GaAs using atomic H assisted MBE

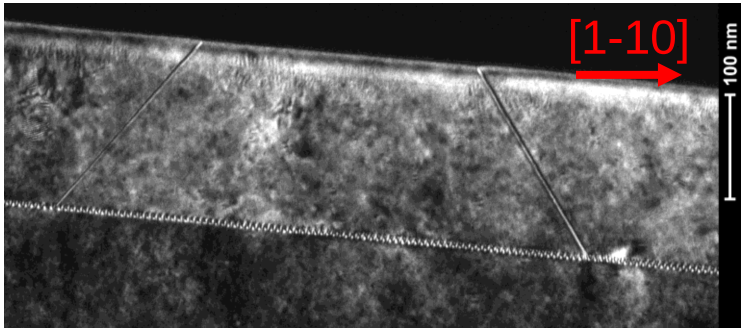
M.Fahed et al, Nanotechnology 27, 505301 (2016)

- Atomic hydrogen flux improves the selectivity of GaSb growth w.r.t. SiO_2 mask

10 nm InAs on 150 nm GaSb inside 100 nm wide apertures;
T_g=470° C*; Sb/Ga=2; V_{Ga}=0,1 ML.s^{-1}*



TEM analysis from G.Patriarche (C2N)

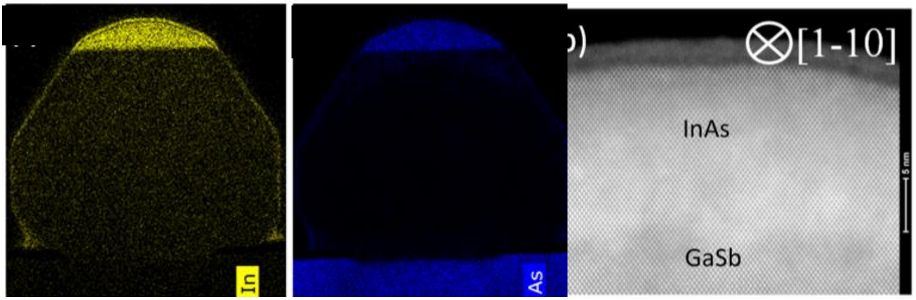


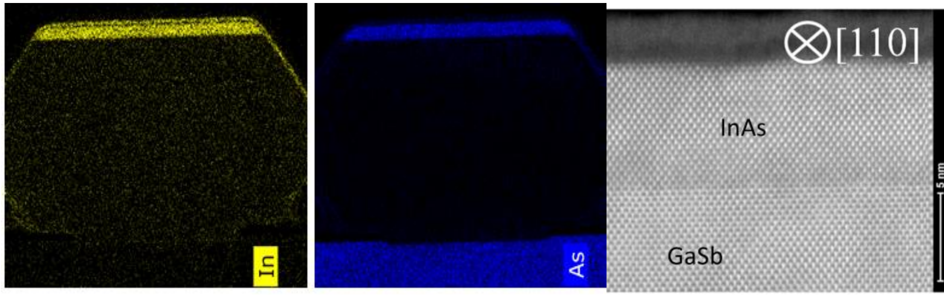
M.Fahed et al, Journal of Crystal Growth (2016)

- TD free relaxed GaSb nanotemplates can be obtained on GaAs (with a few stalking faults)

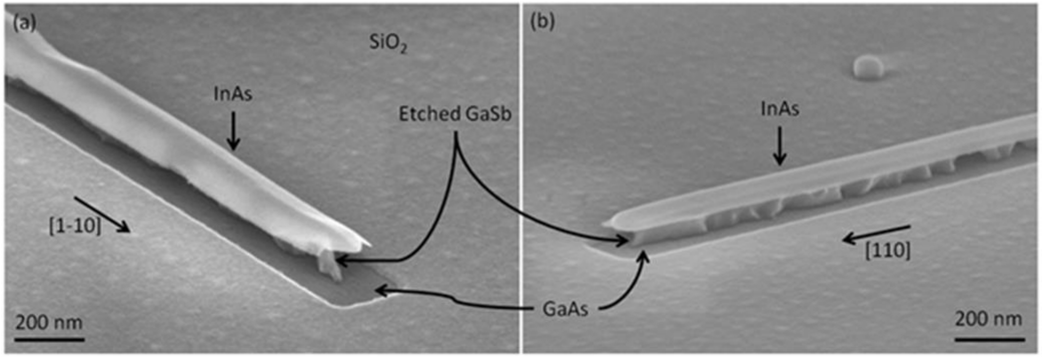
Growth conditions for SA-MBE

InAs on GaSb nanotemplates on GaAs





- ➢ High quality InAs nanowires can be formed on top of the GaSb nanotemplates

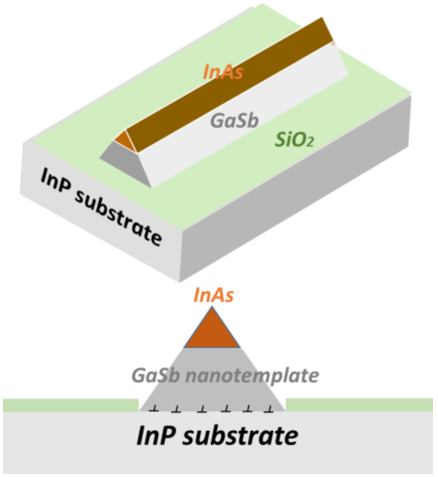


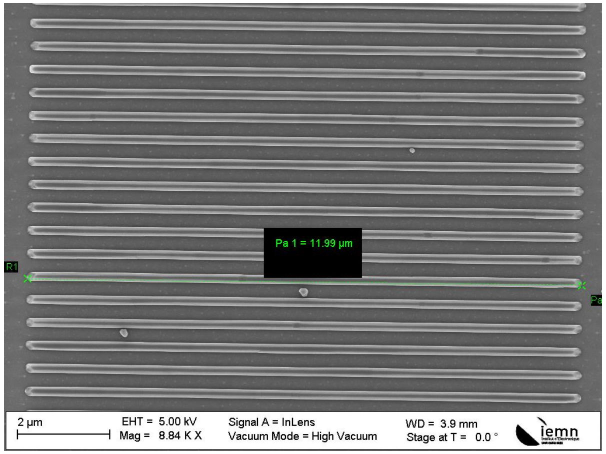
- ➢ InAs NW can be realeased after GaSb selective under-etching (ammonia based solution)

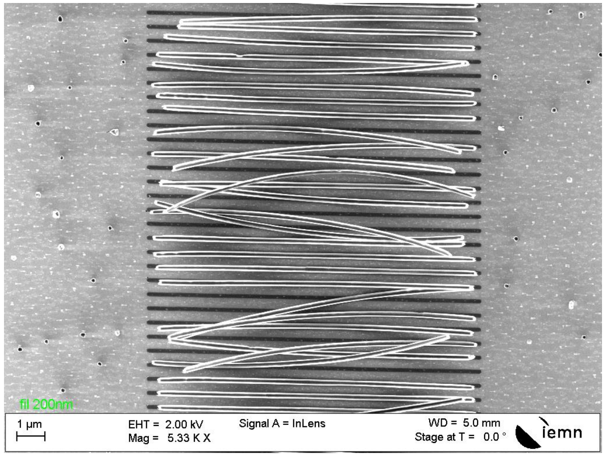
Selective area growth for in-plane nanowire fabrication

InAs NW on GaSb/InP nanotemplates

15 nm InAs on top of 150 nm GaSb grown on InP SI (001) substrate







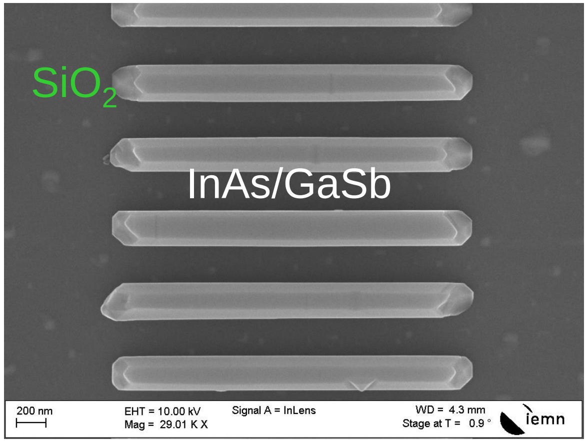
- ⇨ 100 or 200 nm wide / 12 µm long stripes opened in SiO_2 on InP
- ⇨ Deoxidization under As_4 + atomic H fluxes
- ⇨ 150 nm GaSb growth under atomic H with
  $V_{growth}=0.1$ ML.s^{-1}
  Sb/Ga=2
  $T_{growth}=470°$ C
- ⇨ 15 nm InAs ($V_{growth}=0.2$ ML.s^{-1}).

After GaSb selective chemical etching + supercritical drying

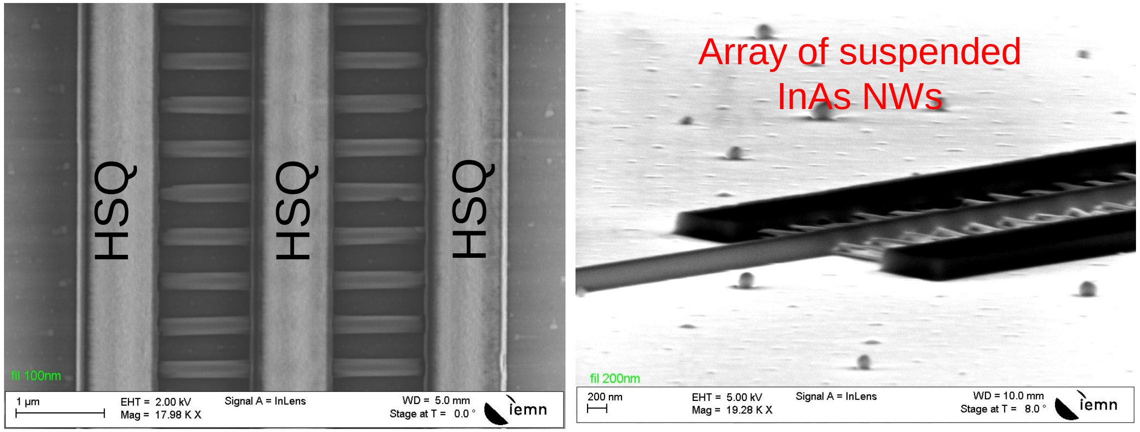
⇨ InAs NWs can be released

Selective area growth for in-plane nanowire fabrication

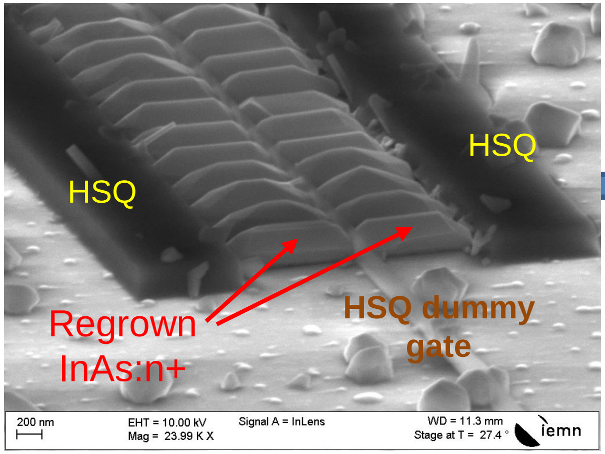
InAs NWs with raised Source and Drain contact on InP



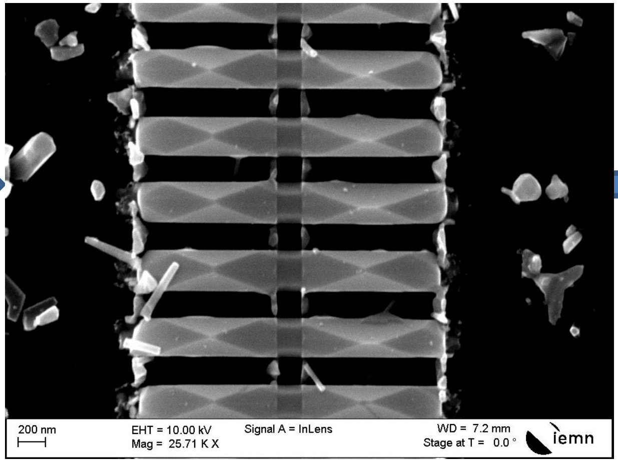
1. Selective growth of InAs (15 nm) / GaSb(150 nm) on InP



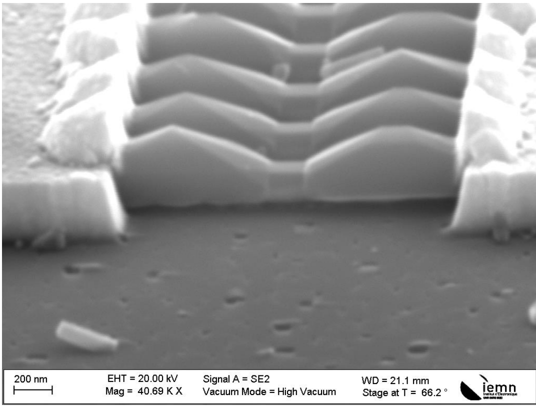
2. HSQ dummy gate and pillars maintaining InAs NWs after development



3. Second regrowth of 150 InAs:Si



4. HSQ removal



5. Metal contacts deposition

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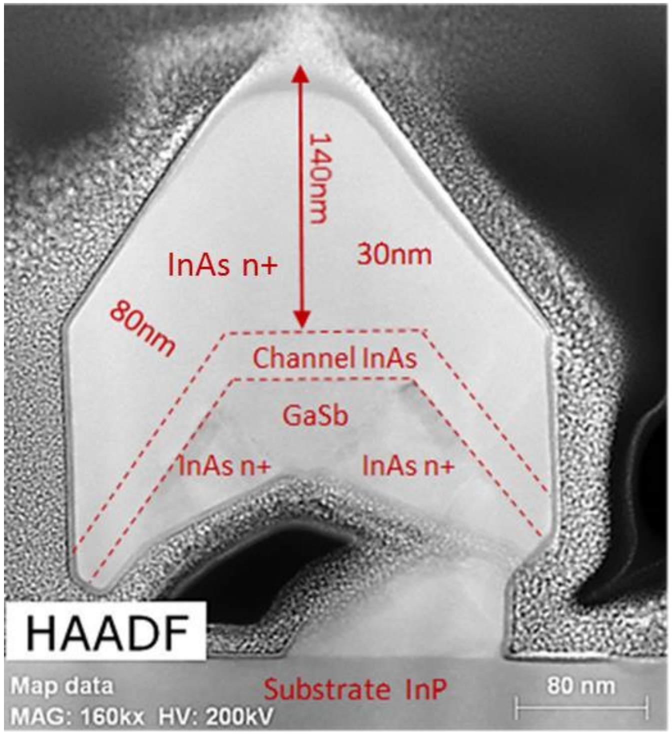
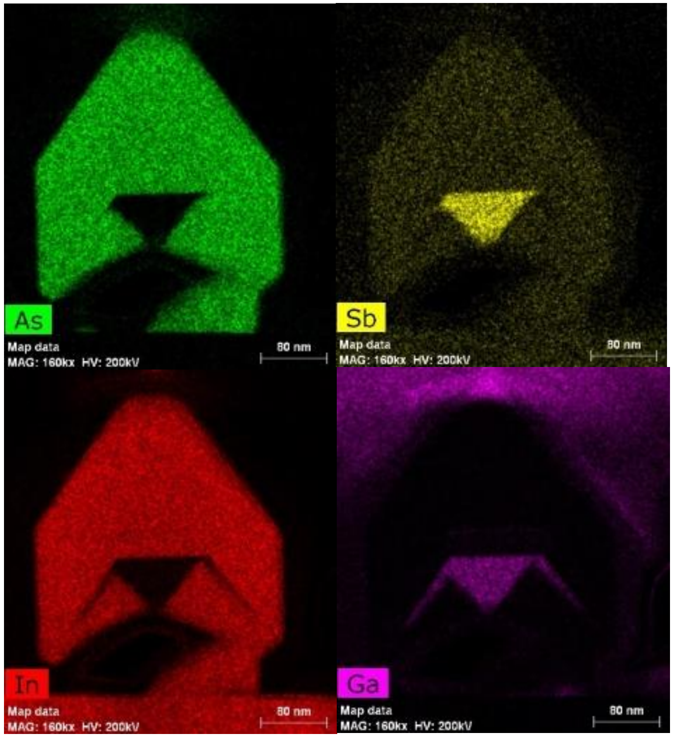
M.Pastorek, PhD Thesis IEMN (2017)

Selective area growth for in-plane nanowire fabrication

InAs NWs with raised Source and Drain contact on InP

HAADF and EDX analysis in the access area
(Collab. A. Addad, UMET)



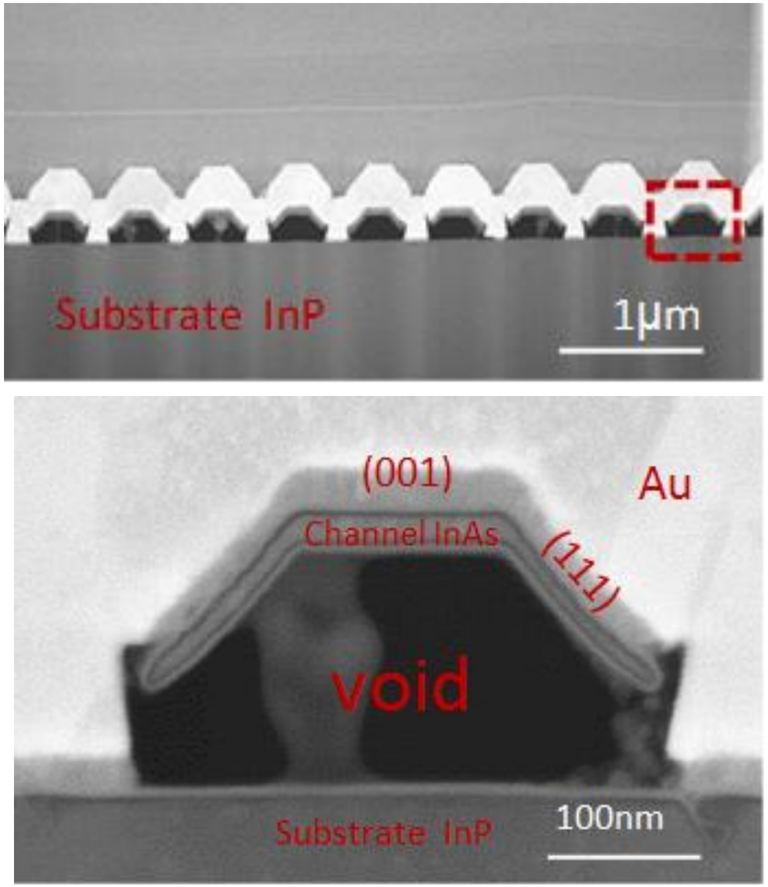


M.Pastorek, PhD Thesis IEMN (2017)

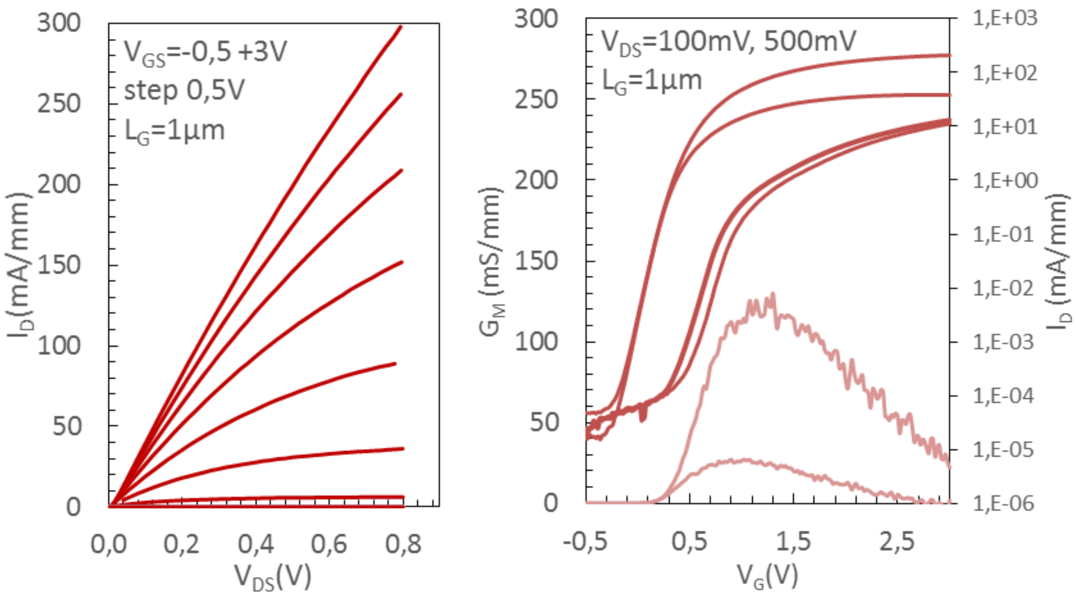
Selective area growth for in-plane nanowire FET

InAs NWs with raised Source and Drain contact on InP

STEM analysis in the channel



Transistor characteristics

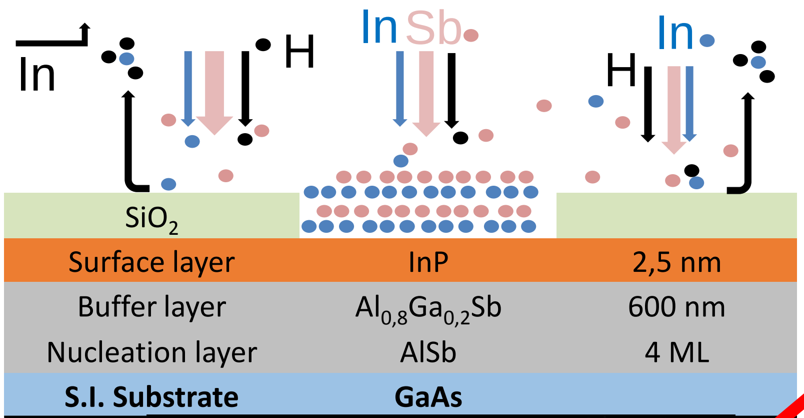


M.Pastorek, PhD Thesis IEMN (2017)

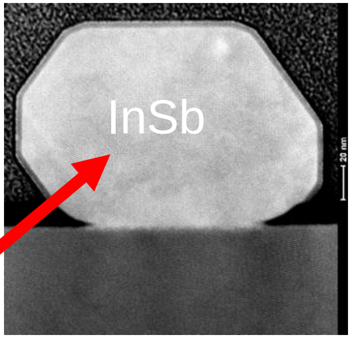
Selective area growth of InSb on GaAs

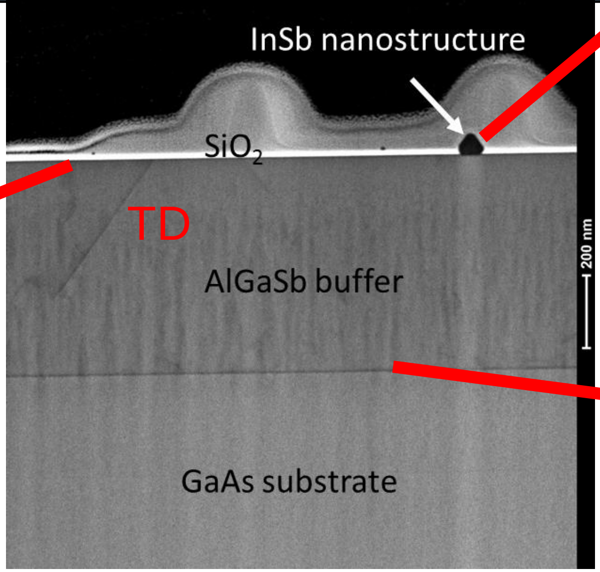
Using AlGaSb buffer

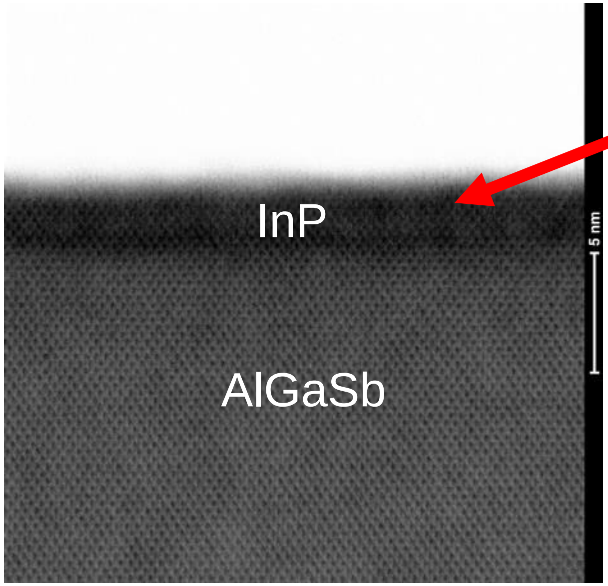
InSb/Al$_{0,8}$Ga$_{0,2}$Sb:
$\Delta a/a \approx 6\%$

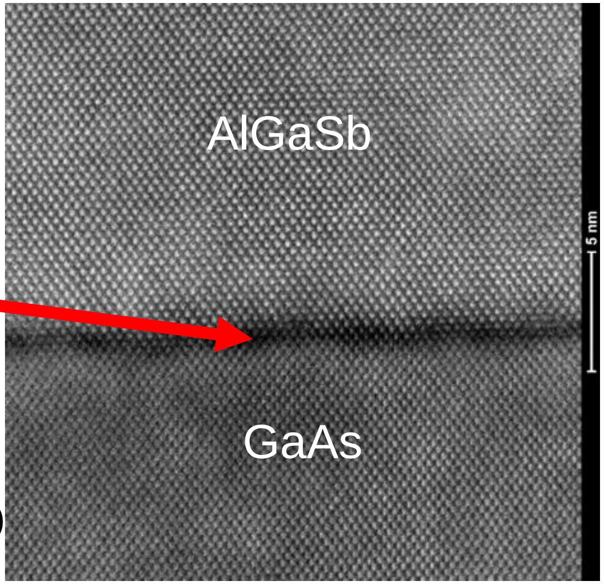


Surface layer	InP	2,5 nm
Buffer layer	Al$_{0,8}$Ga$_{0,2}$Sb	600 nm
Nucleation layer	AlSb	4 ML
S.I. Substrate	**GaAs**	









TEM analysis from G.Patriarche (C2N)

Desplanque et al, Nanotechnology 29 (2018) 305705

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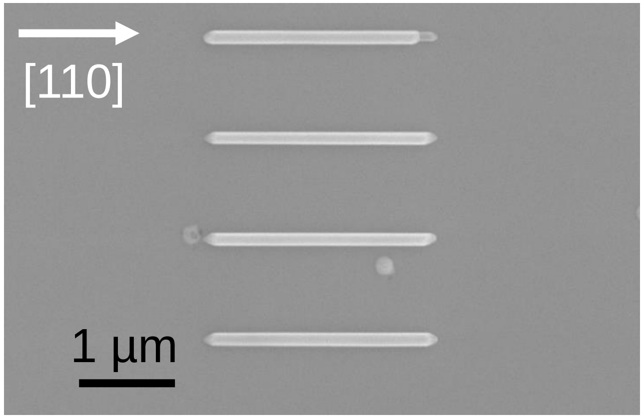
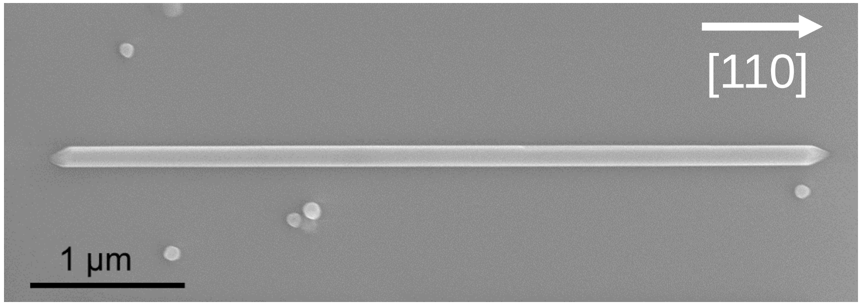
Selective area growth of InSb on GaAs

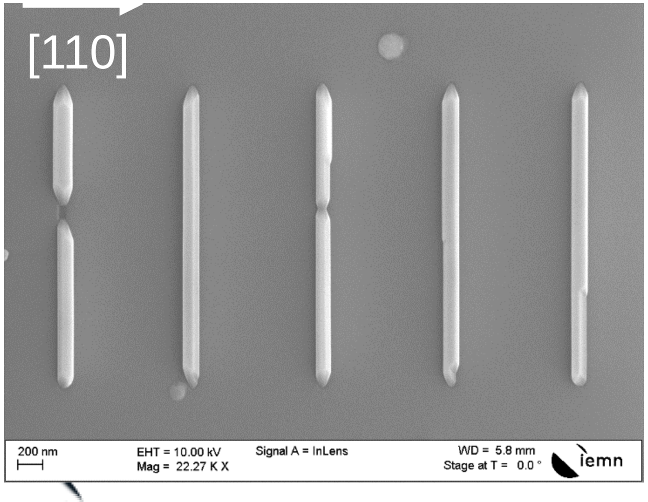
Using AlGaSb buffer

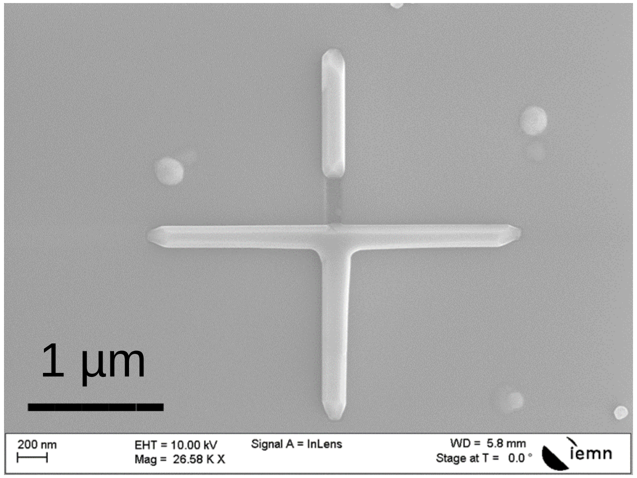


Growth inside 100 nm wide 2,6 µm long apertures



Growth inside 50 nm wide 5 µm long apertures



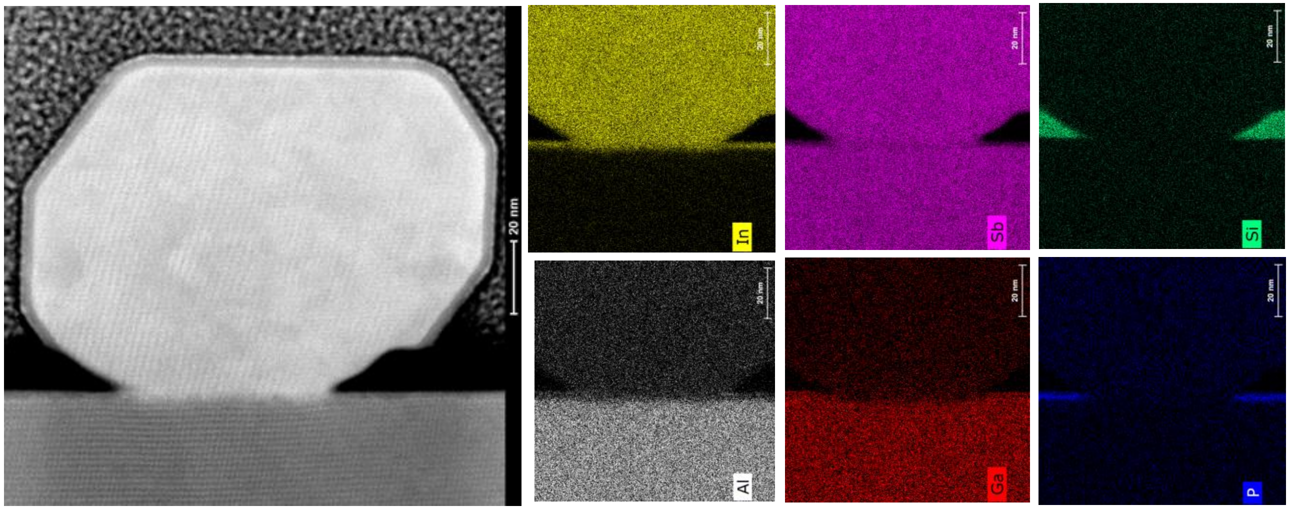


Growth inside 100 nm wide 2,6 µm long cross

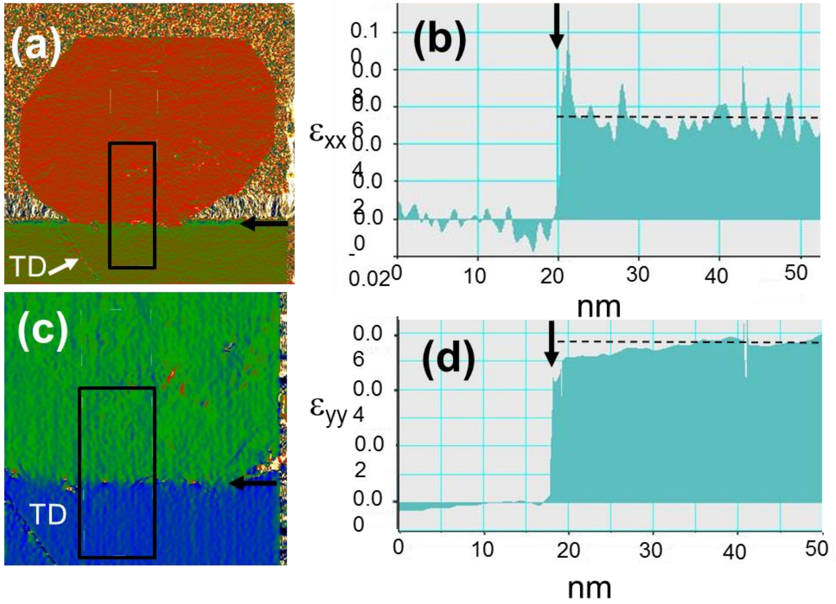
Desplanque et al, Nanotechnology 29 (2018) 305705

Selective area growth of InSb on GaAs

Using AlGaSb buffer



→ P has been removed in the aperture during deoxidization under Sb_2 flux + H



- → Mismatch is accomodated at the regrown interface by misfit dislocations without any TD in the InSb nanostructure
- → Regrown interface more rough than for GaSb/GaAs (effect of P replacement?)

EDX and GPA from G.Patriarche (C2N)

Desplanque et al, Nanotechnology 29 (2018) 305705

Outline

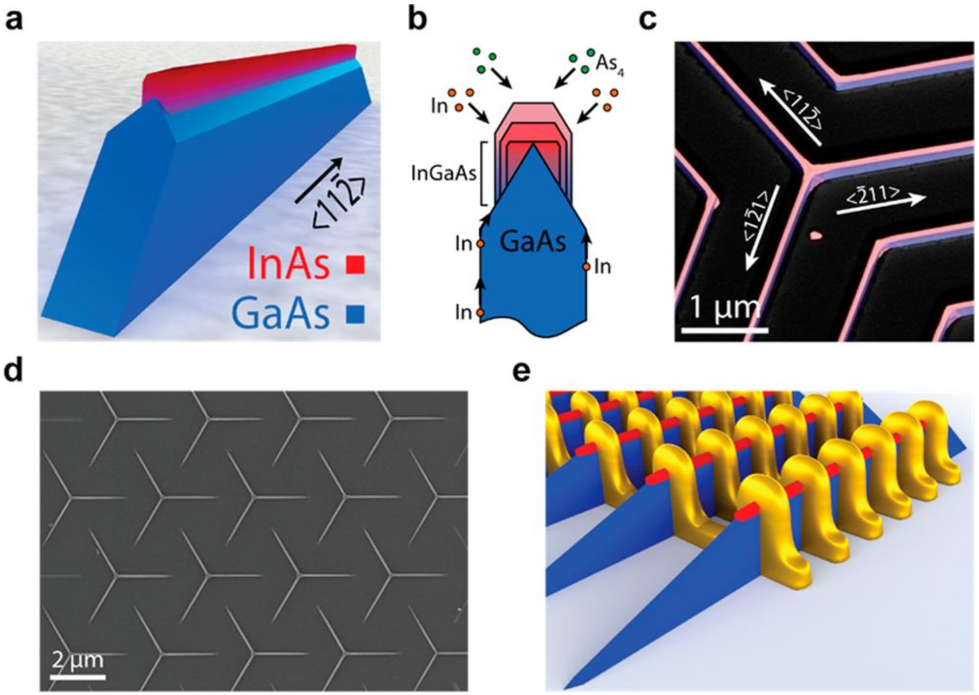
- Selective Area Growth: definition, motivation and method?
- Opportunities for Selective Area Growth (SAG) for III-V nanostructures
  - Optoelectronics
  - III-V MOSFET development
  - Quantum technologies
- Review of SAG developments (mainly MOCVD)
- Development of MBE-SAG for in-plane III-V nanostructures
  - Mask preparation
  - Surface deoxidation
  - Growth conditions
  - Atomic H assisted MBE
  - Examples of III-V nano-SAG using MBE
- Conclusion and prospects

Conclusion

- NanoSAG can address several technological issues
- MOCVD combined to advanced mask preparation using Si technology is the « natural » way but…
- SAG with MBE works also…
- Increasing interest for Selective area grown in-plane nanostructures for quantum technologies…

MBE SAG for quantum devices

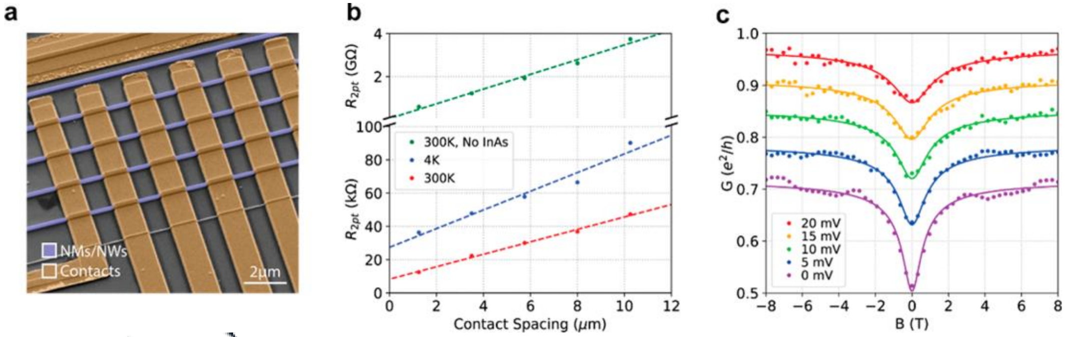
MBE SAG of in-plane InAs NW (EPFL)



→ MBE SAG on GaAs $(111)_B$ substrate masked with SiO_2

→ InAs NW grown on top of GaAs nanomembranes thanks to In migration on side-wall

→ Transport measurements (TLM) reaveal quasi-1D electronic transport

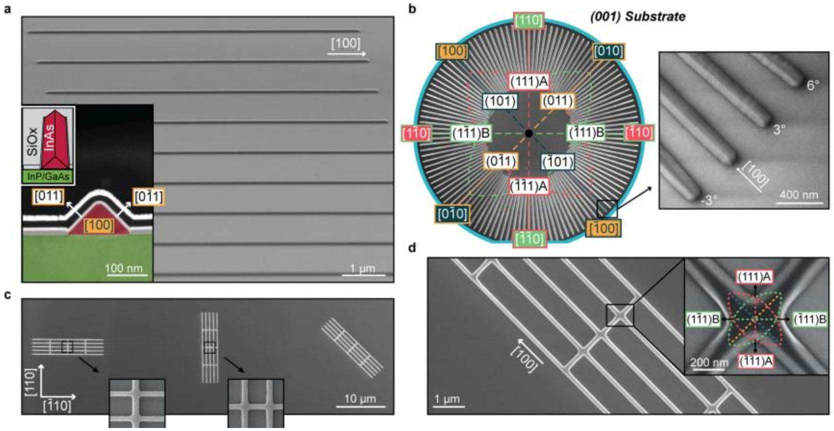


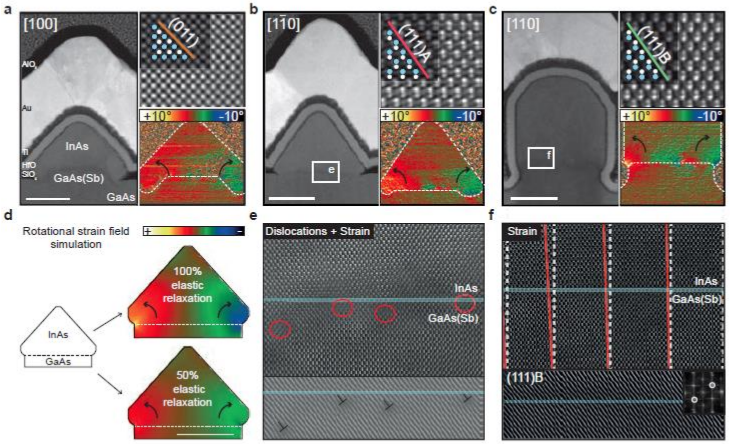
Friedl et al, Nano Lett. 2018, 18, 2666−2671

SAG for quantum devices

SAG-based topological networks (Niels Bohr Institute, QuTech Delft and StationQ)

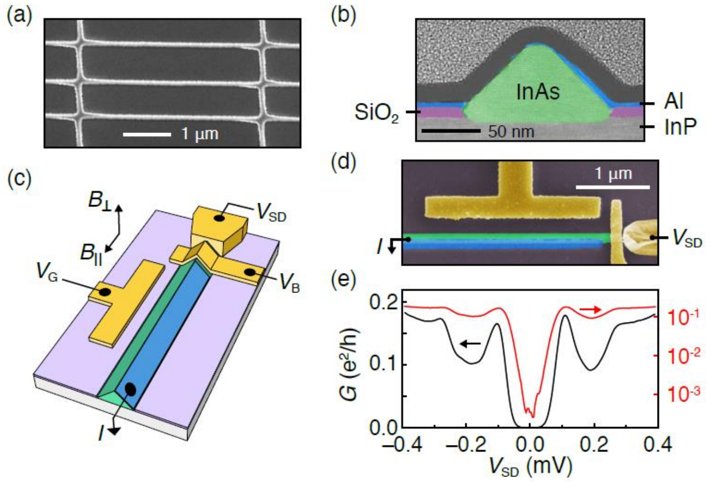
- ➢ SAG of InAs NW networks using MBE



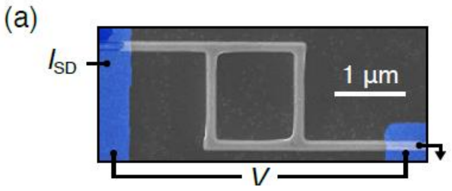


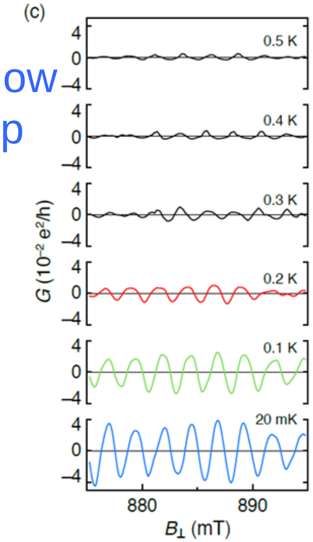
Use of a GaAs(Sb) layer to promote InAs strain relaxation

- ➢ 1D topological superconductors with proximity coupled InAs/Al



- ➢ Quantum interferences at very low temperature in InAs micro-loop





Krizek et al, arXiv:1802.07808v2 *(2018)*
Vaitiekenas et al, arXiv:1802.04210v2 (2018)

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Thank you for your attention…